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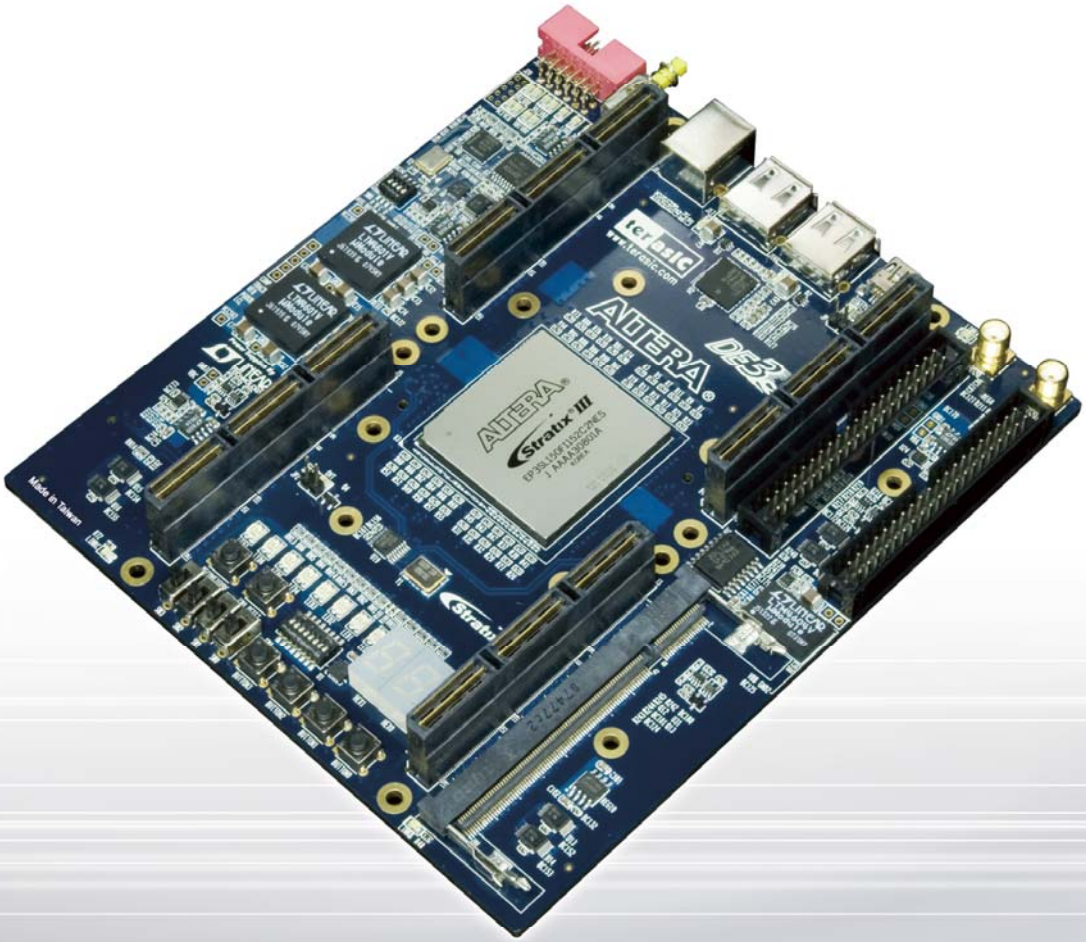


ALTERA®

DE3

Development and Education Board

User Manual

Stratix™III

NiosII

USB
UNIVERSAL SERIAL BUS

CONTENTS

Chapter 1
Overview

This chapter presents the features and design characteristics of the DE3 board.

1.1 Introduction

The DE3 board has plenty of features that allow users to implement a wide range of designed circuits. The Stratix® III device is capable of dealing with resource-consuming projects and complex algorithm verification; the HSTC interface is equipped for high-speed inter-connection and configurable I/O standards. The DDR2 SO-DIMM socket puts the experience of faster memory access into practice, while the SD card socket provides the realization of data storage extension.

In addition, the DE3 board has an innovative stackable mechanism which allows users to assemble DE3 boards into a powerful system as shown in Figure 1.1. The DE3 can also connect with multiple daughter boards designed by Terasic in stock.

Figure 1.1 The stackable mechanism of the DE3 board

1.2 Layout and Components

Figure 1.2 and Figure 1.3 is the top and bottom view of the DE3 board. It depicts the layout of the board and indicates the location of the connectors and key components. Users can refer to this figure for relative location when the connectors and key components are introduced in the following chapters.

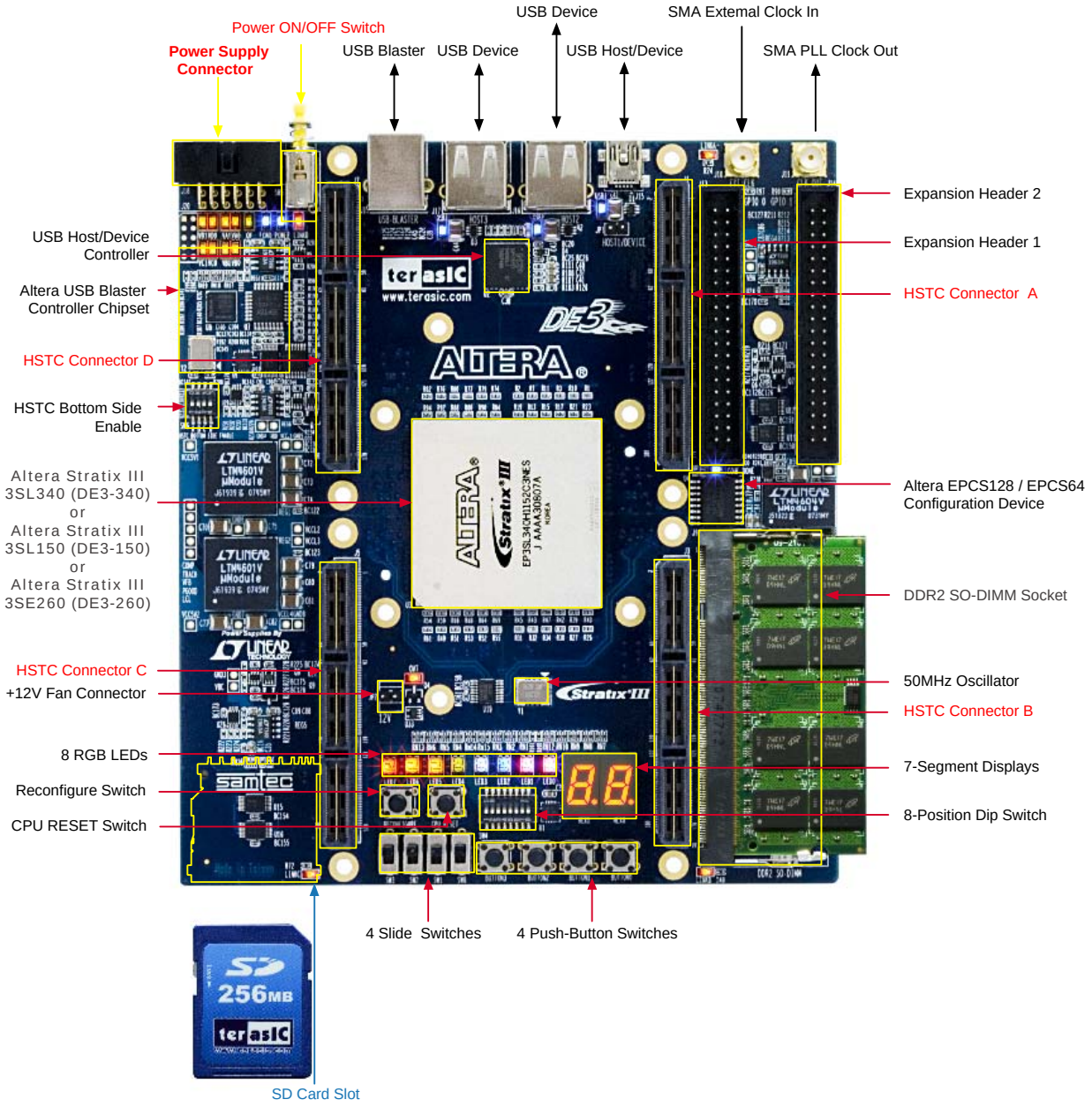


Figure 1.2 The DE3 board (Top view)

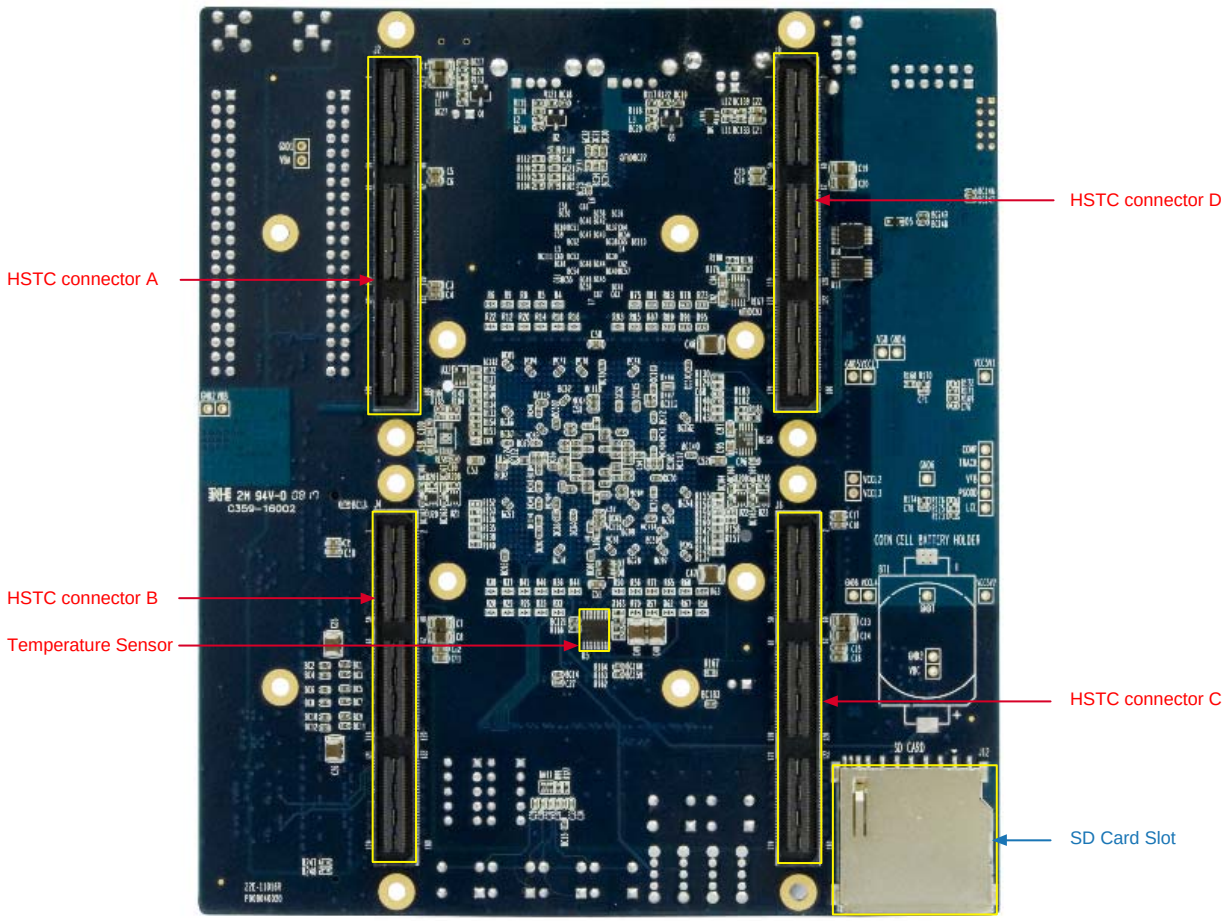


Figure 1.3. The DE3 board (Bottom view)

The following hardware is implemented on the DE3 board:

- Altera Stratix® III FPGA device (3SL340/3SE260/3SL150)
- FPGA configuration interface:
  - Built-in USB Blaster circuit for programming and user API control
  - Altera Serial Configuration device – EPCS128/EPCS64
- Expansion Interface:
  - 8 HSTC connectors
  - Two 40-pin Expansion Headers
- Memory Interface:
  - DDR2 SO-DIMM socket
  - SD Card socket

- User I/O Interface:
  - 4 push-button switches
  - 4 slide switches
  - 1 eight position DIP switch
  - 2 seven-segment displays
  - 8 RGB LEDs
- Clock system
  - One 50MHz oscillator
  - 2 SMA connectors for external clock input and PLL clock output
- Other interface
  - 1 USB Host/Slave controller(1 three-ports USB Host/Device controller)
  - 1 temperature sensor chip for FPGA temperature measurement

1.3 Block Diagram of the DE3 Board

Figure 1.4 shows the block diagram of the DE3 board. To provide maximum flexibility for the users, all key components are connected with the Stratix III FPGA device. Thus, users can configure the FPGA to implement any system design.

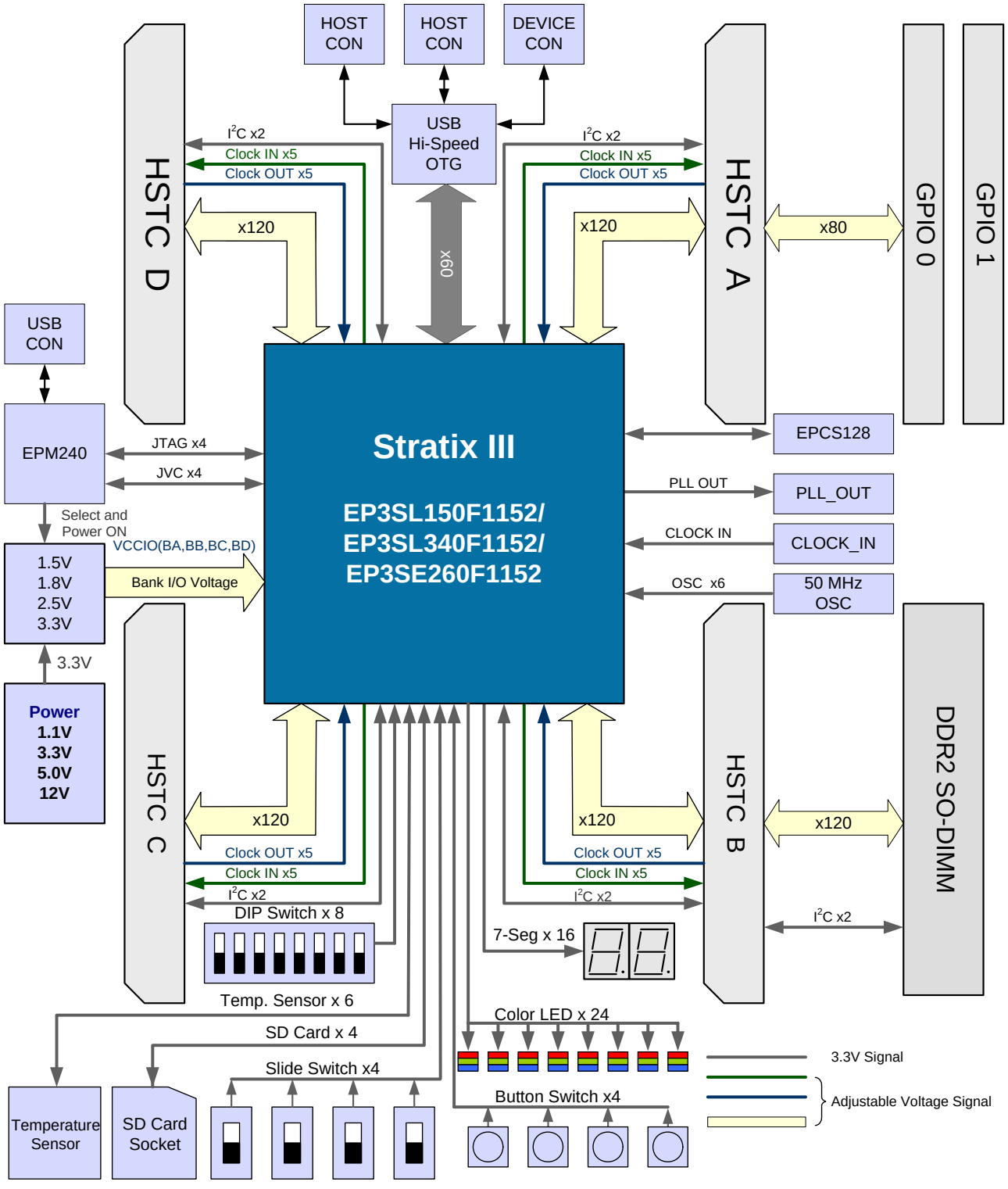


Figure 1.4 Block diagram of the DE3 board

Below is more detailed information regarding the blocks in Figure 1.4:

Stratix III FPGA

- **EP3SL340**
  - 338,000 logic elements (LEs)
  - 18,381K Total Memory Kbits
  - 526 18x18-bit Multipliers blocks
  - 12 phase-locked-loops (PLLs)
  -
- **EP3SE260**
  - 254,400 logic elements (LEs)
  - 16,282K Total Memory Kbits
  - 768 18x18-bit Multipliers blocks
  - 12 phase-locked-loops (PLLs)

- **EP3SL150**
  - 142,000 logic elements (LEs)
  - 6,390K Total Memory Kbits
  - 384 18x18-bit Multipliers blocks
  - 8 phase-locked-loops (PLLs)

Serial Configuration device and USB Blaster circuit

- Altera's EPCS128/EPCS64 Serial Configuration device
- On-board USB Blaster for programming and user API control
- Support JTAG mode

DDR2 SO-DIMM socket

- Up to 4GB capacity
- Share the same I/O bus with HSTC connector B

SD card socket

- Provides SPI and 1-bit SD mode for SD Card access

Push-button switches

- 6 push-button switches
  - 1 CPU Reset
  - 1 FPGA Reconfigure
  - 4 user-defined inputs
- Debounced by a Schmitt trigger circuit
- Normally high; generates one active-low pulse when the switch is pressed

Slide switches

- 4 slide switches for user-defined inputs
- When a switch is set to the DOWN or UP position (i.e., close to or away from the edge of the DE3 board), it causes logic 0 or 1, respectively.

Clock inputs

- 50MHz oscillator
- 1 SMA connector for PLL clock output
- 1 SMA connector for external clock input

USB Host/Slave controller

- Complies fully with Universal Serial Bus Specification Rev. 2.0
- Support data transfer at high-speed, full-speed, and low-speed
- Support both USB host and device
- Three USB ports (one type mini-AB for host/device and two type A for host)
- Support Nios II with the Terasic driver
- Support Programmed I/O (PIO) and Direct Memory Access (DMA)

Eight 180-pin High Speed Terasic Connectors (HSTC) expansion headers

- 4 male and 4 female connectors are on the top and the bottom of DE3 board, respectively.
- 240 LVDS pairs of user-defined IO pins
- Configurable I/O voltage for 3.3V, 2.5V, 1.8V, and 1.5V

Two 40-pin expansion headers

- 72 FPGA I/O pins, as well as 8 power and ground lines, are brought out to two 40-pin expansion connectors
- 40-pin header is designed to accept a standard 40-pin ribbon cable used for IDE hard drives
- Share the same I/O pins with HSTC connector A

Chapter 2
Using the DE3 Board

This chapter gives instructions for using the DE3 board and its components.

It is strongly recommended that users should read the *Getting Started with the Altera DE3 board.pdf* before using the DE3 board. The document is located in the *DE3_usermanual* folder on the **DE3 System CD**. The contents of the document includes following:

1. Purpose of the DE3 Board
2. Scope of the DE3 Board and Supporting Material
3. Installing the Altera Design Software
4. Obtain a License File from Altera's website
5. Setup the License File for Terasic Power Controller IP.
6. Install the USB Blaster Driver
7. Power up the DE3 Board
8. Programming the FPGA Device on the DE3 Board

2.1 Configuring the FPGA and Serial Configuration Device

■ **Programming the FPGA device:**
The DE3 board has a built-in USB Blaster circuit, which allows users to program the FPGA device using USB cable and Quartus II programmer in JTAG mode. Current configuration will be lost when the power is turned off.

To download a configuration bit stream into the Stratix III FPGA, perform the following steps:

- Make sure that power is provided to the DE3 board
- Connect the USB cable supplied to the USB Blaster port of the DE3 board (see Figure 2.1)
- The FPGA can now be programmed in the Quartus II Programmer by selecting a configuration bit stream file with the *.sof* filename extension.

Please refer to *Getting Started with the Altera DE3 board.pdf* for more detailed procedure of FPGA programming.

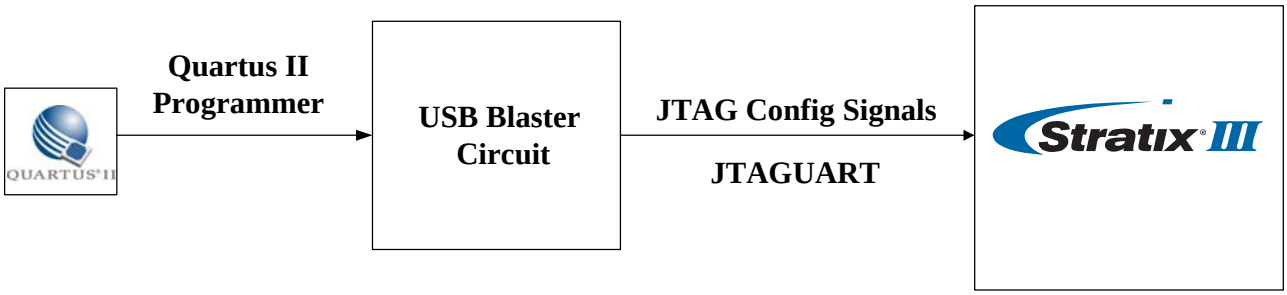


Figure 2.1 The JTAG configuration scheme

■ **Programming the serial configuration device :**

The DE3 board contains a serial configuration device (U4) that stores configuration data for the Stratix III FPGA. This configuration data is automatically loaded from the serial configuration device chip into the FPGA when the board is powered up.

Since the *Active Serial* programming interface is not supported on the DE3 board, users will need to use a Serial Flash Loader (SFL) function to program the serial configuration device via the JTAG interface. The FPGA-based SFL is a soft intellectual property (IP) core within the FPGA that bridges the JTAG and flash interfaces. The SFL mega-function is available from Quartus II software. Figure 2.2 shows the programming method when adopting a SFL solution.

Please refer to *Appendix C Programming the Serial Configuration device* for the basic programming instruction on the serial configuration device. More detailed information on the SFL mega-function can be found in *Altera Application Note 370: Using the Serial Flash Loader With the Quartus II Software.*

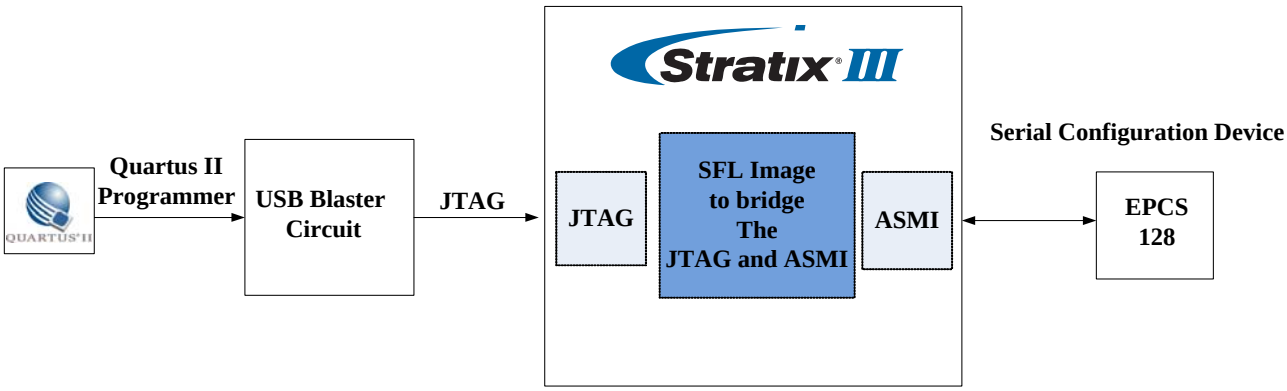


Figure 2.2. Programming a serial configuration device with the SFL solution

2.2 JTAG Chain

This section describes how to setup the JTAG chain on DE3 board.

If the DE3 board is used without any board connected and all the positions in SW6 are switched to OFF (i.e., down position), the JTAG-interface signals of all HSTC connectors are bypassed, as shown in Figure 2.3.

When the top HSTC connector is not connected with any daughter board, the JTGA interface is bypassed. If a daughter board is connected to the top HSTC connector, the JTAG interface will be enabled automatically. Figure 2.4 shows the JTAG chain with a daughter board connected to the DE3 board via top HSTC connector A. Note that if the daughter board does not use the JTAG interface, the TDI and TOD pins on the daughter board must be shorted for the JTAG signals to pass through.

A four position DIP switch (SW6) on DE3 board is used to control the JTAG interface signals of bottom HSTC connectors. Table 2-1 indicates the detailed configurations of SW6. When the bottom connector is connected with other DE3 board or an daughter board, users need to configure the SW6 to connect the JTAG chain to other board accordingly. Figure 2.5 shows there are two DE3 boards stacked, and the JTAG chain is established through HSTA connector A, as shown in Figure 2.6.

Table 2-1. DIP switch (SW6) setting for JTAG interface on bottom HSTC connectors

Position	Switch Setting	
	Turn OFF (lower position)	Turn ON (upper position)
1	Bypass the JTAG interface on the Bottom HSTC connector A(J2)	Enable the JTAG interface for Bottom HSTC connector A(J2)
2	Bypass the JTAG interface on the Bottom HSTC connector B(J4)	Enable the JTAG interface for Bottom HSTC connector B(J4)
3	Bypass the JTAG interface on the Bottom HSTC connector C(J6)	Enable the JTAG interface for Bottom HSTC connector C(J6)
4	Bypass the JTAG interface on the Bottom HSTC connector D(J8)	Enable the JTAG interface for Bottom HSTC connector D(J8)

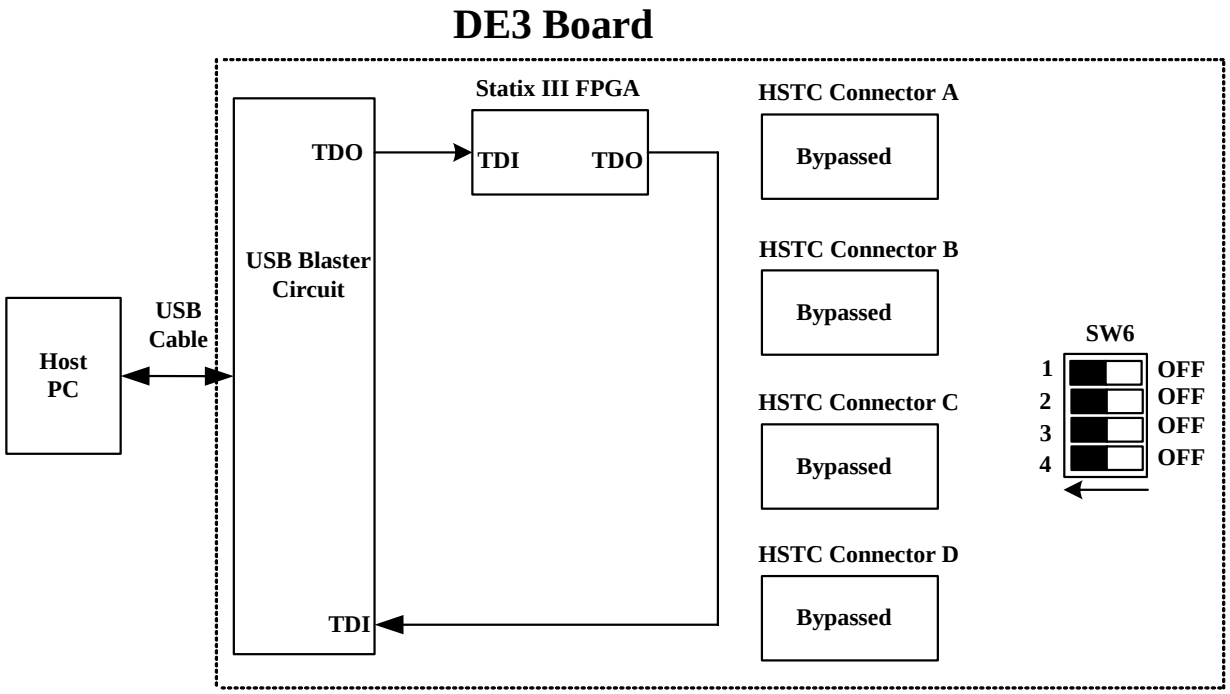


Figure 2.3. JTAG chain for a standalone DE3 board

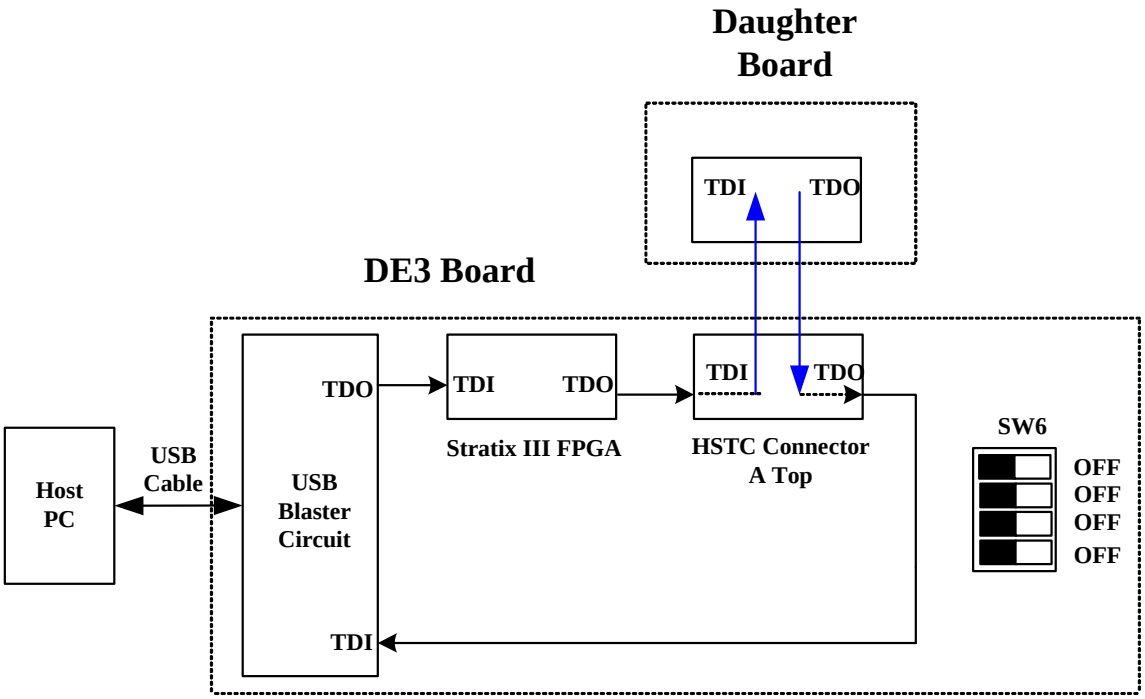


Figure 2.4. JTAG chain for a daughter board connected with DE3 board via top HSTC connector A

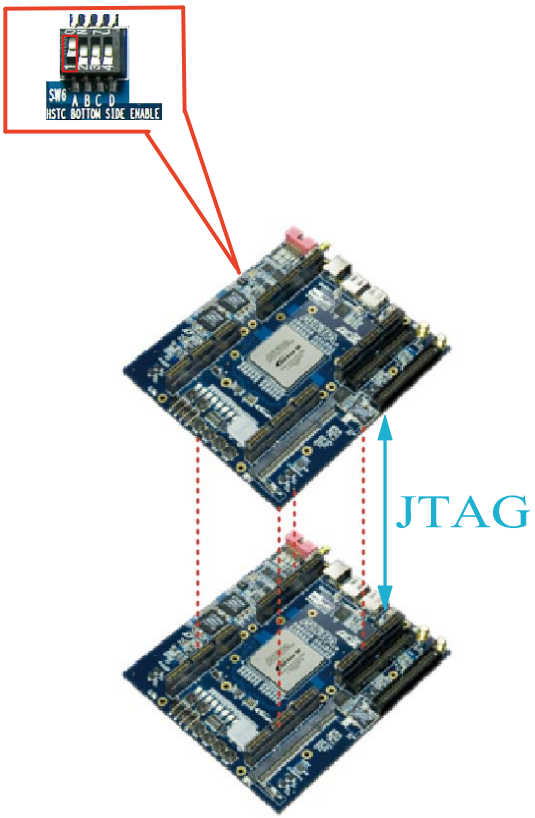


Figure 2.5. The two DE3 boards stacked and the JTAG path is established through HSTC connector A.

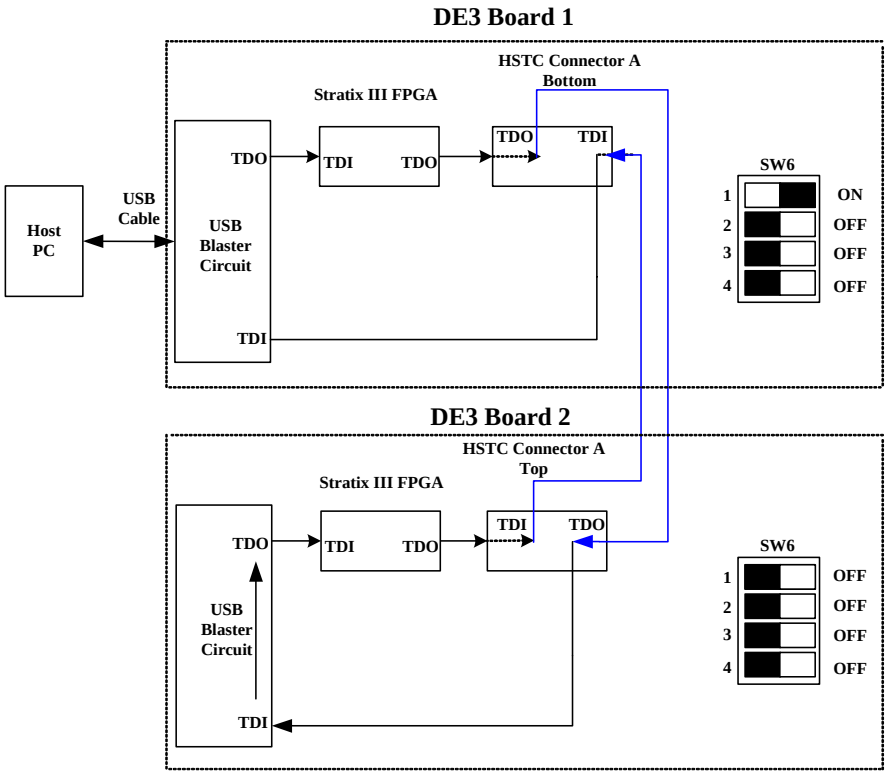


Figure 2.6. JTAG chain for two stacked DE3 boards

2.3 Using the User I/O Interface

- **Push-Button Switches:**

The DE3 board provides four user-defined, one CPU reset, and one Reconfigure push-button switches. The Reconfigure push-button is used to force a re-boot of the FPGA from the serial configuration device.

The CPU reset push-button is an input to the Stratix III device. It is intended to be the master reset signal for the FPGA designs loaded into the Stratix III device. The CPU reset push -button is connected to the DEV_CLRn pin on the FPGA. The DEV_CLRn setting is a pin option in the Quartus II software that users must enable to function the CPU reset as DEV_CLRn instead of a standard I/O.

Each of these switches is de-bounced using a Schmitt Trigger circuit, as indicated in Figure 2.7. Each push-button provides a high logic level (3.3 volts) or a low logic level (0 volts) when it is not pressed or pressed, respectively. Table A-1 shows the connections between the push-buttons and the FPGA.

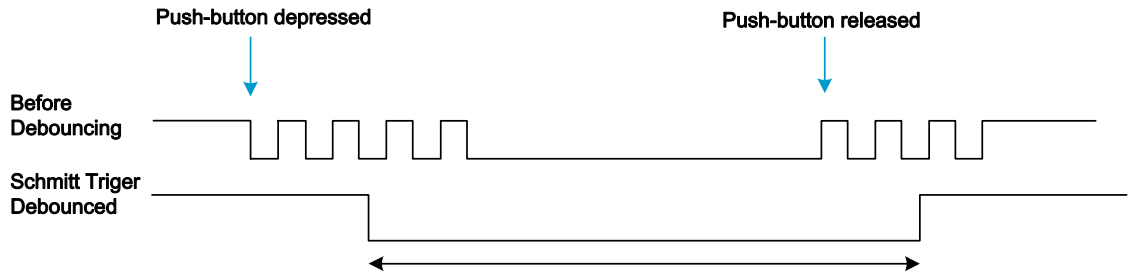


Figure 2.7. Switch debouncing

- **Slide Switches and DIP Switch**

There are also four slide switches and one 8-position DIP switch on the DE3 board. Each switch is connected directly to a pin of the Stratix III FPGA. When a slide switch is in the DOWN position (i.e., closest to the edge of the board) or the UP position, it provides a low logic level (0 volts) or a high logic level (3.3 volts) to the FPGA, respectively. For 8-position DIP switch, when a switch is in the DOWN position (closest to the edge of the board) or the UP position, it provides a high logic level (3.3 volts) or a low logic level (0 volts) to the FPGA. The connections between the slide switches and the FPGA are shown in Table A-2, whereas Table A-3 shows the connections between the 8-position DIP switch and the FPGA.

- **RGB LEDs**

There are 8 RGB user-controllable LEDs on the DE3 board. Each LED has red, green, and

blue color, driven directly by the Stratix III FPGA; The LED is turned on or off when the associated pins are driven to a low or high logic level, respectively. A list of the pin names on the FPGA that are connected to the RGB LEDs is given in Table A-4.

■ **7-Segment Displays**

The DE3 board has two 7-segment displays. As indicated in the schematic in Figure 2.8, the seven segments are connected to pins of the Stratix III FPGA. Applying a low or high logic level to a segment to light it up or turns it off.

Each segment in a display is identified by an index listed from 0 to 6 with the positions given in Figure 2.9. In addition, the decimal point is identified as DP. Table A-5 shows the mapping of the FPGA pin assignments to the 7-segment displays.

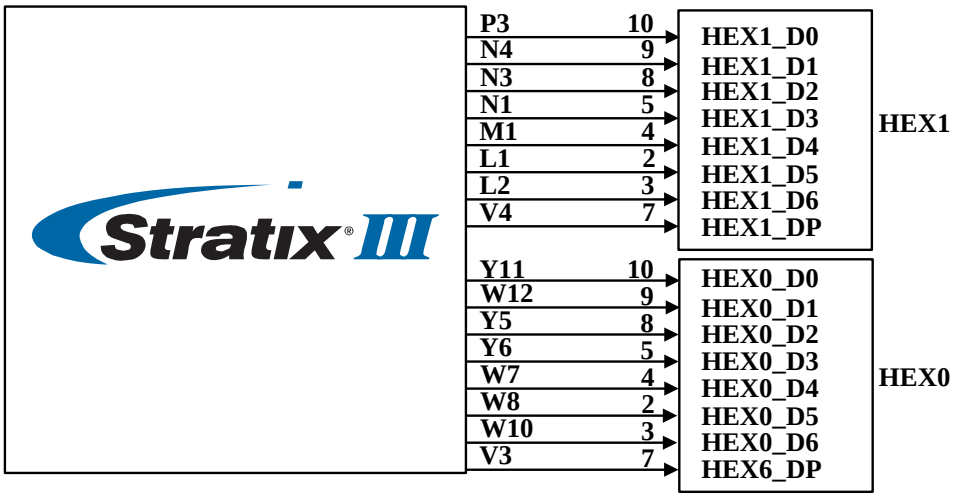


Figure 2.8. Connection between 7-segment displays and Stratix III FPGA

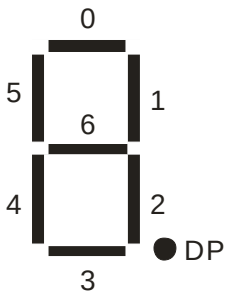


Figure 2.9. Position and index of each segment in a 7-segment display

2.4 I/O Groups and V_{CCIO} Control Circuit

Most of the user-defined I/O pins on Stratix III device are used for connectors. They are divided

into four I/O groups, named A, B, C and D. Table 2-2 shows the relation between I/O groups and connectors.

Table 2-2 The relation between I/O groups and connectors

I/O Group	Connectors
A	HSTC connector A, GPIO expansion headers *(1)*
B	HSTC connector B, DDR2 SO-DIMM socket *(2)*
C	HSTC connector C
D	HSTC connector D

Note:

(1): HSTC connector A and GPIO expansion headers share the same I/O pins.

(2): HSTC connector B and DDR2 SO-DIMM socket share the same I/O pins.

Besides, the V_{CCIO} level for these I/O groups of the FPGA can be configured, and many I/O standards are supported. The I/O standard of each I/O group on DE3 board has to be set through a software utility named "**DE3 System Builder**". Such tool is intended to generate a top level Quartus II project, which includes the power controller IP.

After the FPGA is programmed, the power controller IP will control the V_{CCIO} control circuit to provide desired V_{CCIO} and V_{CCPD} level to the FPGA, according to I/O standard selected by users as indicated in Figure 2.10.With this feature, users can not only confirm if the V_{CCIO} level meets the design requirement, but also reduce the chance of the DE3 board and its daughter cards being damaged.

Please refer to *Stratix III handbook chapter 7. Stratix III Device I/O Features* for more information about the I/O standard and voltage levels of the Stratix III device. There will be more instructions for **DE3 System Builder** in Chapter 4.

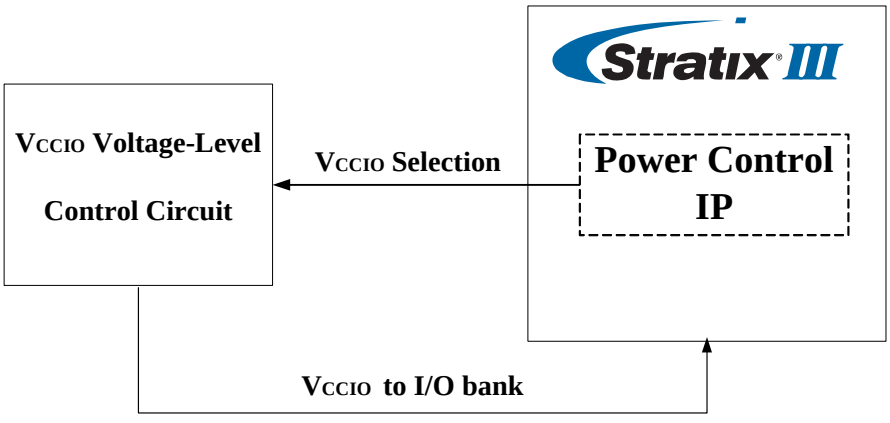


Figure 2.10. The architecture of Power Control IP and V_{CCIO} control circuit

Finally, there are LEDs located at the left-top corner of the DE3 board to indicate the VCCIO voltage level of each I/O group, as shown in Figure 2.11. For example, the LED VA1 and VA2 will be turned on and off, respectively, when the VCCIO of I/O Group A is set to 2.5V. Please refer to Table 2-3 for the status of the LED indicator.

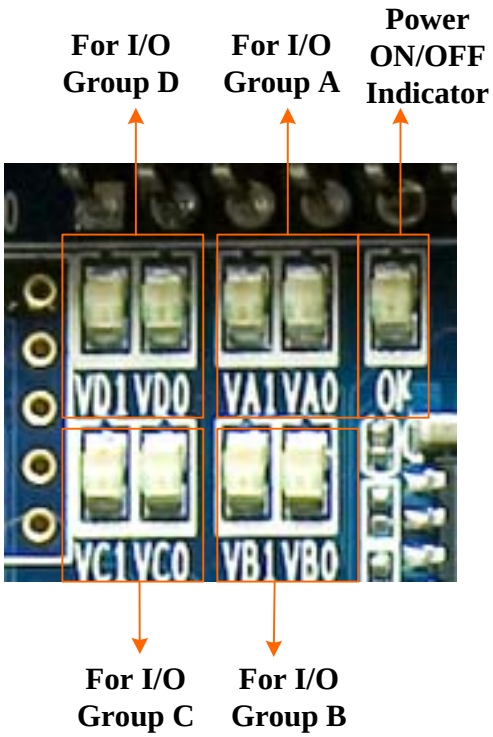


Figure 2.11. The Voltage-Level Indicator for the I/O Groups

Table 2-3 The LEDs indicates the VCCIO voltage level of each IO Group.

LED / VCCIO	Vx1*(1)*	Vx0*(1)*	OK
3.3V	Light ON	Light ON	Light ON
2.5V	Light ON	Light OFF	Light ON
1.8V	Light OFF	Light ON	Light ON
1.5V	Light OFF	Light OFF	Light ON
0V	Light OFF	Light OFF	Light OFF

Note:

(1): Vx1 can be VA1, VB2, VC3, and VD1; Vx0 can be VA0, VB0, VC0, and VD0

2.5 Using the HSTC Connectors

The High Speed Terasic Connector (HSTC) is a high speed expansion interface defined by Terasic Technologies. The DE3 board is equipped with 8 HSTC connectors (J1 ~ J8), which can be used to connect the Stratix III FPGA with daughter boards or the other DE3 boards. The detailed specifications of the HSTC connector are described below:

- **4 HSTC Connector Groups:**
  The eight HSTC connectors on the DE3 board are divided into 4 groups: HSTC A, HSTC B, HSTC C, and HSTC D. Each group has a male and female HSTC connector on the top and bottom side of the DE3 board, respectively. In addition, both the male and female HSTC connector shares the same I/O pins except JTAG and I2C interface.

- **I/O Distribution:**
  Each HSTC connector has 120 single-ended I/O (60 pair differential channels), 10 single-ended IO with 5 each for clock input and output (2 differential clock input and output channel), JTAG and I2C bus. In addition, there are three banks on a HSTC connector. The I/O pins used in differential transceiver channels on bank 1 support true LVDS inout. On bank 2 and 3, the I/O pins used in differential transmitter channels support emulated LVDS via a termination resistor, and the differential receiver channels support true LVDS, as shown in. Figure 2.12. In addition, there is a software utility named "**DE3_HSTC**" which can perform the connection test between the I/O pins of the HSTC connector and Stratix III FPGA. The detailed information about this utility can be found in Appendix D : DE3_HSTC Utility.

- **Configurable I/O Standards:**
  The I/O pins of the HSTC connector support many I/O standards with different voltage level, as the V_{CCIO} supplied to FPGA bank I/O is configurable. Users can choose the I/O standard of HSTC connector in the software utility "**DE3 System Builder**".

- **Compatible with HSMC Connector :**
  The HSTC connector is not only designed to be backward-compatible with the HSMC products, but also provides more I/O pins for further connection. The pin assignments of bank 1 and 2 are exactly the same. The only difference between the HSMC and HSTC connector is the pin assignments for bank 3. For HSTC connector, all the I/O pins on the bank 3 are well defined. Figure 2.13 shows the I/O distribution of the bank3 for the HSTC and HSMC connector. Table B-1 shows the pin compatible list for HSTC and HSMC connector.

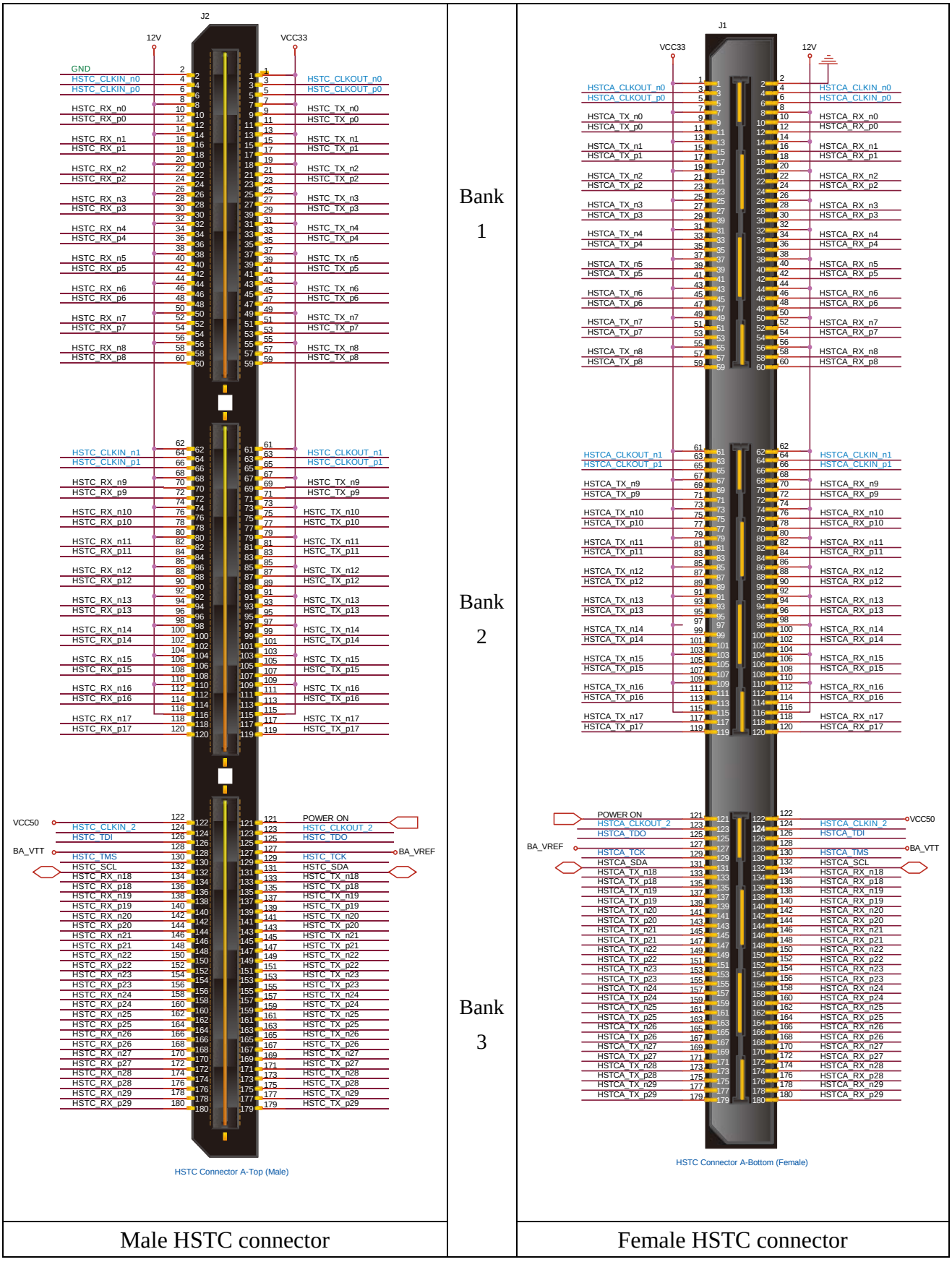
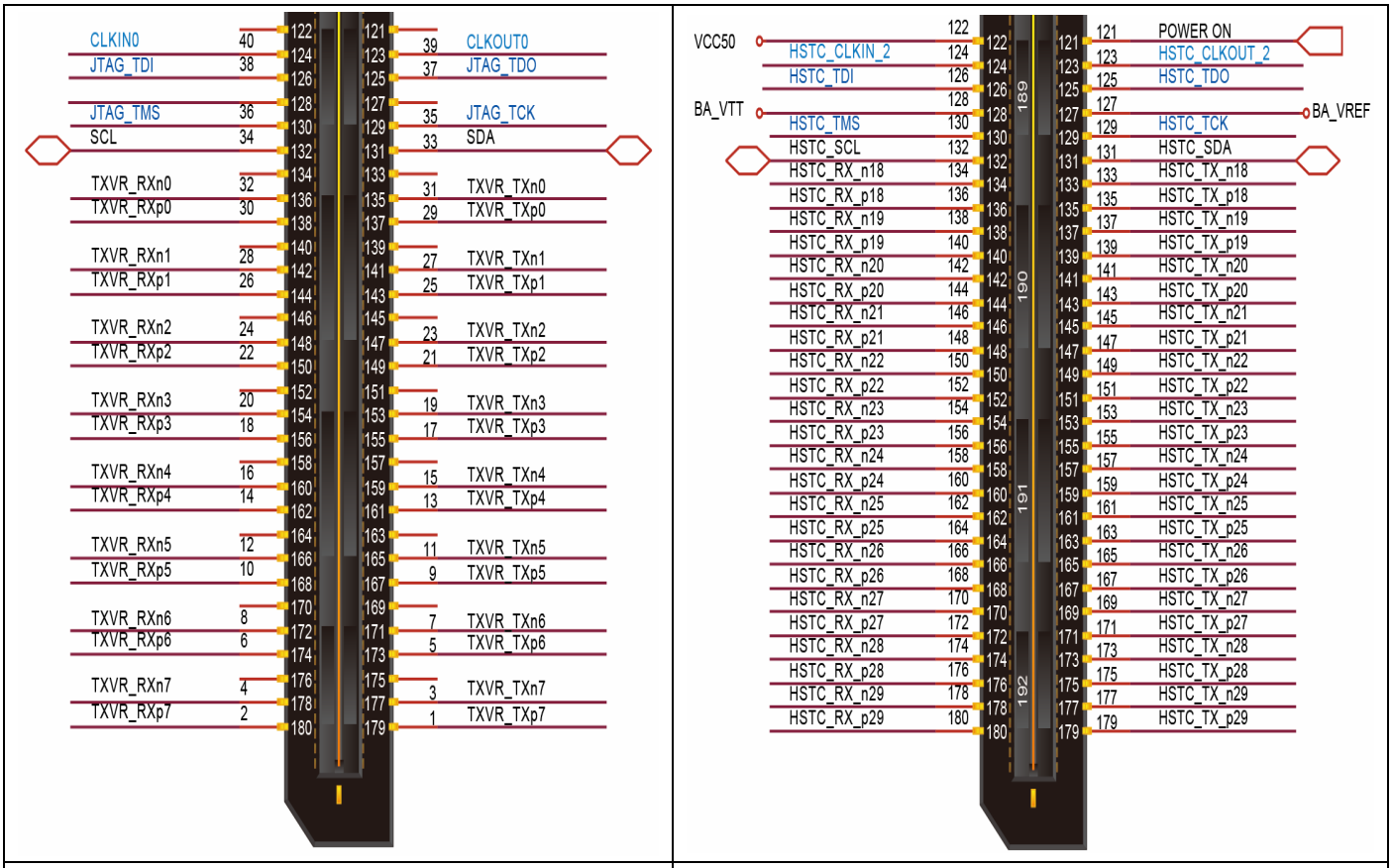


Figure 2.12. The male and female HSTC connectors

- **Share the same I/O pins with other connectors:**
  The HSTC connector group HSTCA (J1, J2) and HSTCB (J3, J4) share the same I/O pins with the GPIO expansion headers (J13, J14) and DDR2 SO-DIMM socket (J9), respectively. Hence none of the combinations above is allowed to be used at the same time.

- **Power Supply:**
  The HSTC connector provides 12, 5, and 3.3 volt for power supply purpose. There are also two power input pin named B<*HSTC Group*>_VTT and B<*HSTC Group*>_VREF, which are connected to the input reference voltage(V_{REF}) and termination voltage pin (V_{TT}) of the Stratix III FPGA, respectively.

Finally, Table A-6 to Table A-11 shows the connections between the HSTC connectors and the FPGA.



HSMC	HSTC

Figure 2.13. The difference between the HSMC and HSTC connectors

2.6 Using the GPIO Expansion Headers

The DE3 Board provides two 40-pin expansion headers as shown in Figure 2.14. Each header has 36 pins connected to the Stratix III FPGA, and the two headers share the same I/O pins with HSTC connector A. The other 4 pins provide DC +5V (VCC5), DC +3.3V (VCC33), and two GND pins. Among these 36 I/O pins, there are 4 pins connected to the PLL clock input and output pins of the FPGA.

The I/O pins on the expansion headers have a great flexibility in selecting the I/O standards. The voltage level of the V_{CCIO} can be configured as 3.3V, 2.5V, 1.8V, or 1.5V.

Finally, Figure 2.15 shows the connections between the GPIO expansion headers and Stratix III. The pin assignments are given in Table A-12 and Table A-13.

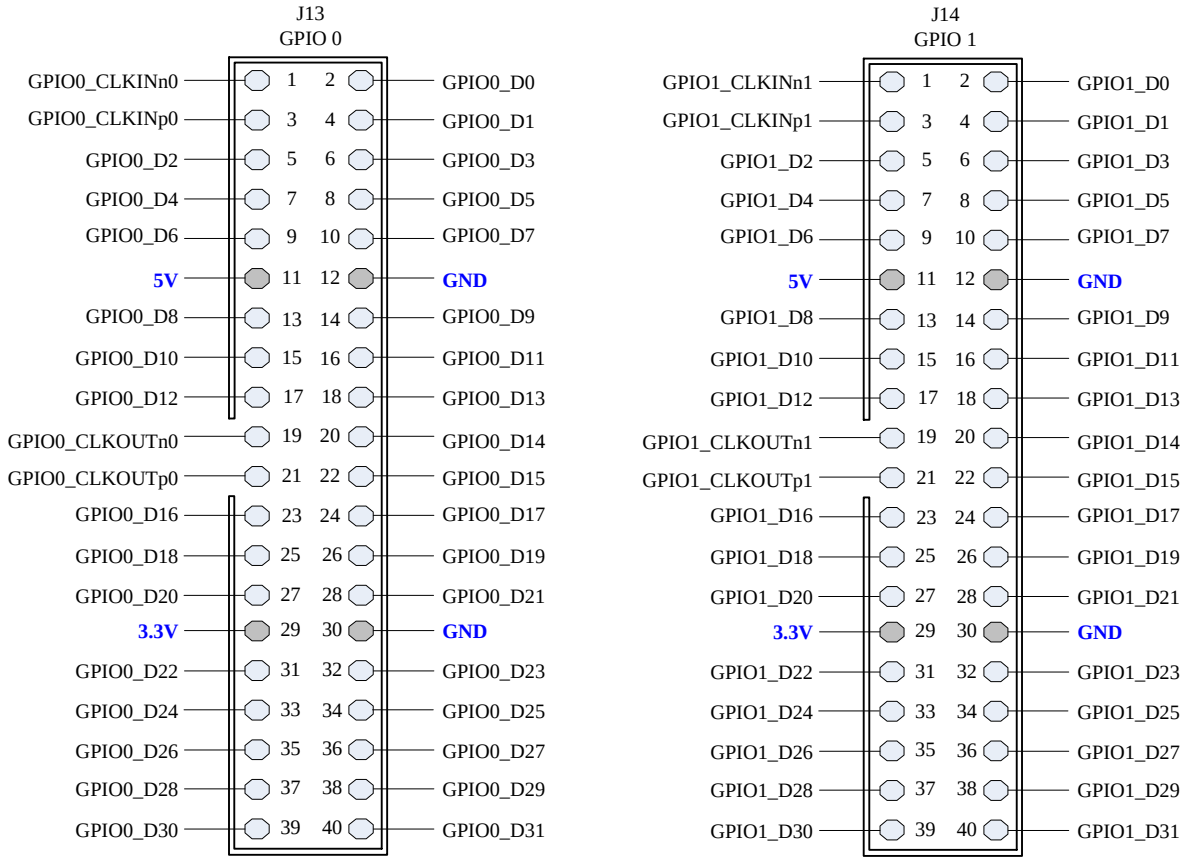


Figure 2.14. Pin distribution of the GPIO expansion headers

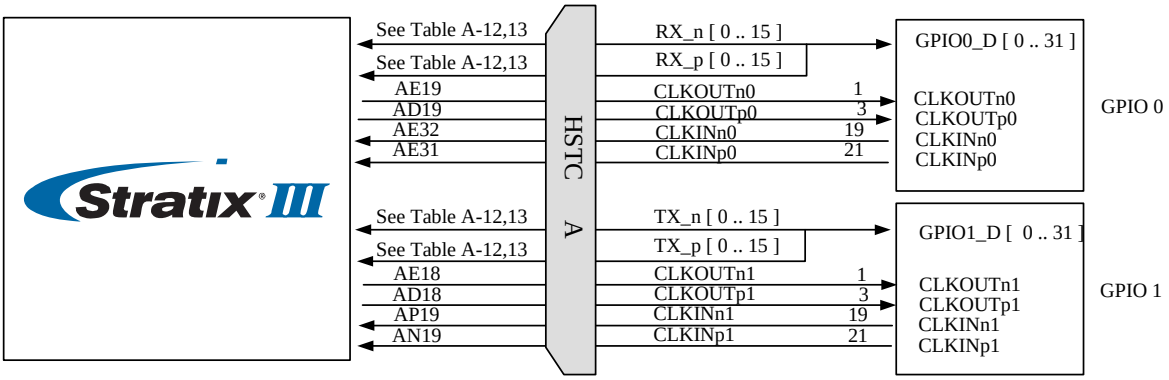


Figure 2.15. Connections between the GPIO expansion headers and Stratix III

2.7 Using the DDR2 SO-DIMM

The DE3 board provides a 200-pin DDR2 SO-DIMM socket. The maximum capacity supported is 4GB. The DDR2 SO-DIMM shares the same I/O pins with the HSTC connector B, except the command input signals *DDR2_CS_N[1..0]* and presence-detect address input signals *DDR2_SA[1..0]*. Users should never use the DDR2 SO-DIMM socket and the HSTC connector B at the same time. Figure 2.16 shows the connections between the DDR2 SO-DIMM socket and Stratix III device. The pin assignments are listed in Table A-14.

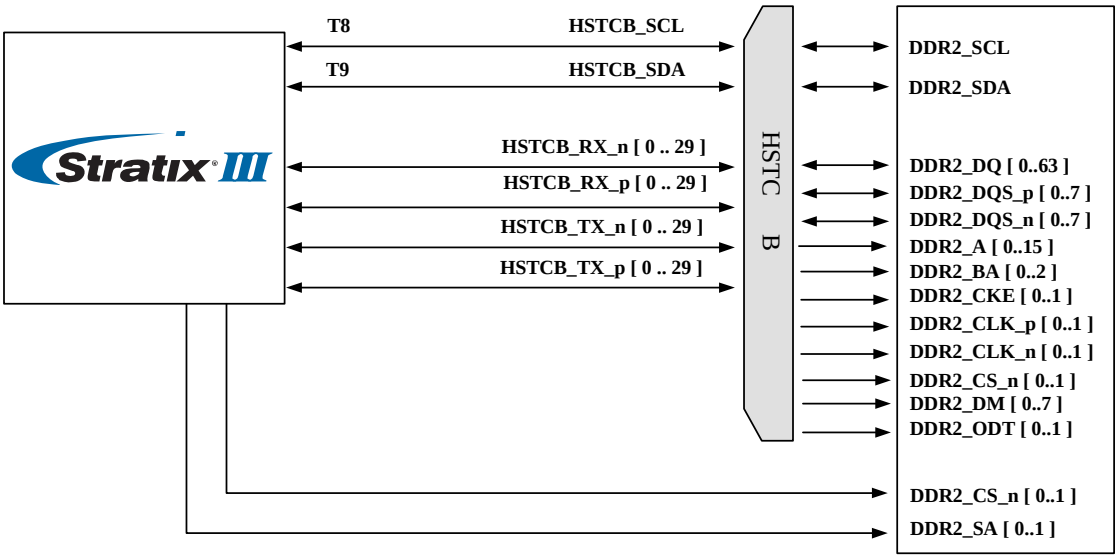


Figure 2.16. Connections between the DDR2 and Stratix III FPGA

2.8 Using the USB OTG

The DE3 board provides both USB host and device interfaces using the Philips ISP1761ET single-chip USB controller. The host and device controllers are compliant with the Universal Serial Bus Specification Rev. 2.0, supporting data transfer at high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s). Figure 2.17 shows the connection between the USB OTG and Stratix III device. The port 1 can be configured as a downstream port, or an upstream port or OTG port. If the port 1 is configured as an OTG port, users can use JP1 to specify host or peripheral role, as listed in Table 2-4. The pin assignments for the associated interface are listed in Table A-15.

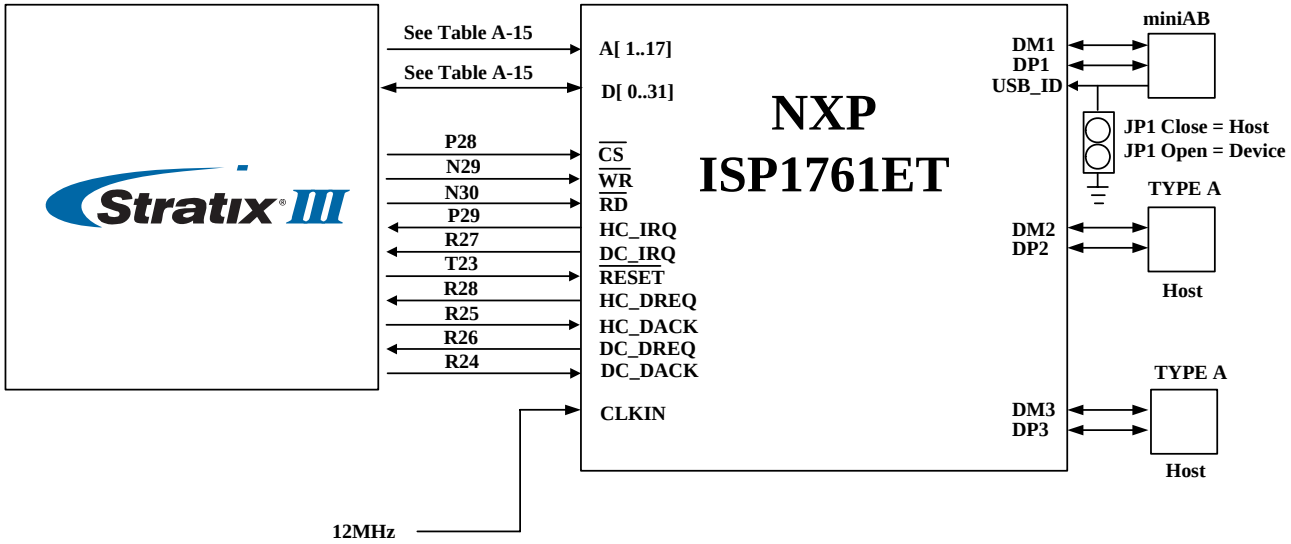


Figure 2.17. Connections between the USB OTG and Stratix III device

Detailed information of the ISP1761ET device can be found in its datasheet and programming guide; both documents are available from the manufacturer's web site, or in the *Datasheet/USB* folder of the **DE3 System CD**. Two complete examples for host and device applications each, can be found in Sections 5.1and 5.2. These demonstrations provide software drivers for the Nios II processor.

Table 2-4 The default host or peripheral setting for port 1 (J15) of the ISP1761ET

JP1 setting	Connectors
Open	Port1 set to peripheral
Close	Port 1 set to host

2.9 Using the SD Card

The DE3 board has a SD card socket and can be accessed as optional external memory in both SPI and 1-bit SD mode. Table A-16 shows the pinout of the SD card socket with Stratix III FPGA.

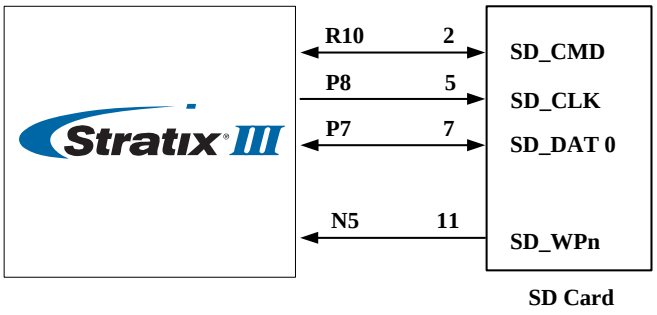


Figure 2.18. Connections between the SD card and Stratix III

2.10 LED Indicators

The DE3 board includes some LEDs to indicate the specified hardware status. The relationship of LED names and their associated functions are list in Table 2-5.

Table 2-5 Description for LED indicator

LED Name	Descriptions
POWER	Light on when Power switch(SW5) is turned on
CONF_DONE	Light on when the configuration data is received by Stratix III FPGA without error ad initialization cycle starts.
LOAD	Light on when USB blaster circuit transmits or receives data
LINKA	Light on when HSTC connector A top (J1) is connected with an extended board
LINKB	Light on when HSTC connector B top (J3) is connected with an extended board
LINKC	Light on when HSTC connector C top (J5) is connected with an extended board
LINKD	Light on when HSTC connector D top (J7) is connected with an extended board
OVT	Light on when the temperature value of the FPGA is higher than the threshold value setting in the temperature sensor.
USB3, USB2, USB1	Power LED indicators for USB port3 (J17), port2 (J16), and port1 (J1). Each LED will be on as soon as the port power of the respective port is enabled by software, for example, after loading drivers

2.11 Clock Circuitry

- **Clock inputs:**

The clock input source of Stratix III FPGA comes from the clock buffer, HSTC connectors, GPIO expansion headers, and SMA connector as indicated in Figure 2.19. Most of these clock inputs are connected to the dedicated high speed clock input pins of the FPGA, which allows users to use any of these clocks as a source clock for the PLL circuit.

- **Clock outputs:**

The clock output of Stratix III FPGA includes HSTC connectors, GPIO expansion headers, SMA connector, and SD card socket as shown in Figure 2.19.

The associated pin assignments for clock buffer and SMA connectors to FPGA I/O pins are shown in Table A-17.

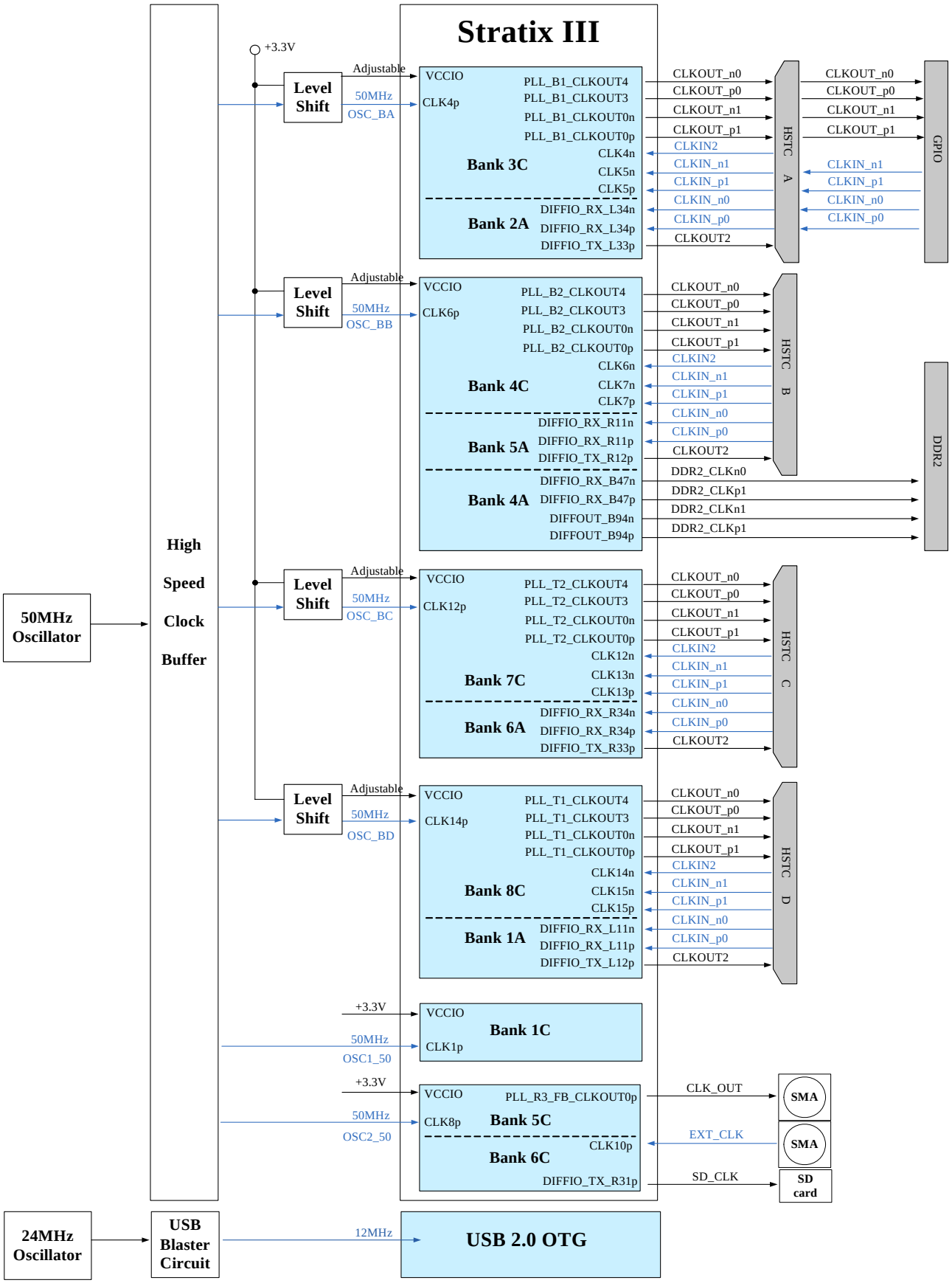


Figure 2.19. Clock connections of the DE3

2.12 Using the Temperature Sensor

The DE3 board is equipped with a temperature sensor MAX1619, which provides temperature sensing and over-temperature alert. These functions are achieved by connecting the temperature sensor to the internal temperature sensing diode of the Stratix III device. The temperature status and alarm threshold registers of the temperature sensor can be programmed by a two-wire SMBus, which is connected to the Stratix III FPGA as shown in Figure 2.20. In addition, the 7-bit POR slave address for this sensor is set to '0011000'.

There is an option of connecting a 2-pin +12V fan to JP2 for cooling purpose. The pin near the HSTC connector C is for +12V, the other one is used for GND. When the temperature of the FPGA device is over the threshold value set by users, the fan will be turned on. The pin assignments for the associated interface are listed in Table A-18.

Finally, the detailed information of the temperature sensor device can be found in its datasheet, which is available from the manufacturer's web site, or in the *Datasheet/Temperature_Sensor* folder of the **DE3 System CD**.

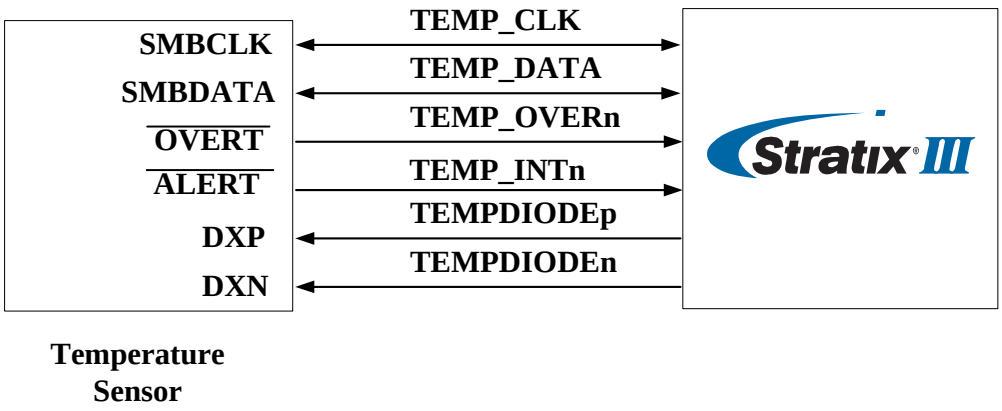


Figure 2.20. Connections between the temperature sensor and Stratix III device

Chapter 3
Control Panel

The DE3 board comes with a PC-based Control Panel that allows users to access various components onboard. The host computer communicates with the board via USB port. The tool can be used to verify the functionality of components.

This chapter presents some basic functions of the Control Panel, illustrates its structure in block diagram form, and finally describes its capabilities.

3.1 Control Panel Setup

The Control Panel software utility is located in the directory "*/Tool/DE3_control_pane/SW*" in the **DE3 System CD**. To execute the program, simply copy the whole folder to your host computer and launch the control panel by double clicking the "*DE3_Control_Panel.exe*".

The *DE3_Control_Panel.exe* will auto-detect the FPGA and download the control codes, the *.sof* and *.elf* file, to the Stratix III device through USB-Blaster port.

To activate the Control Panel, perform the following steps:

1. Make sure Quartus II and NIOS II are installed successfully on your PC.
2. Connect the supplied USB cable to the USB Blaster port and the supplied power cord to J18. Turn the power switch ON as shown in Figure 3.1.
3. Start the executable *DE3_control_panel.exe* on the host computer. Figure 3.2 will appear and the Control Panel starts to auto-detect the FPGA and download the .sof and .elf files.
4. After the configuration file is programmed to the DE3 board, the FPGA device information will be displayed on the window.
5. Note the Control Panel will occupy the USB port, users will not be able to download any configuration file into the FPGA before you exit the Control Panel program.
6. The Control Panel is now ready, as shown in Figure 3.3

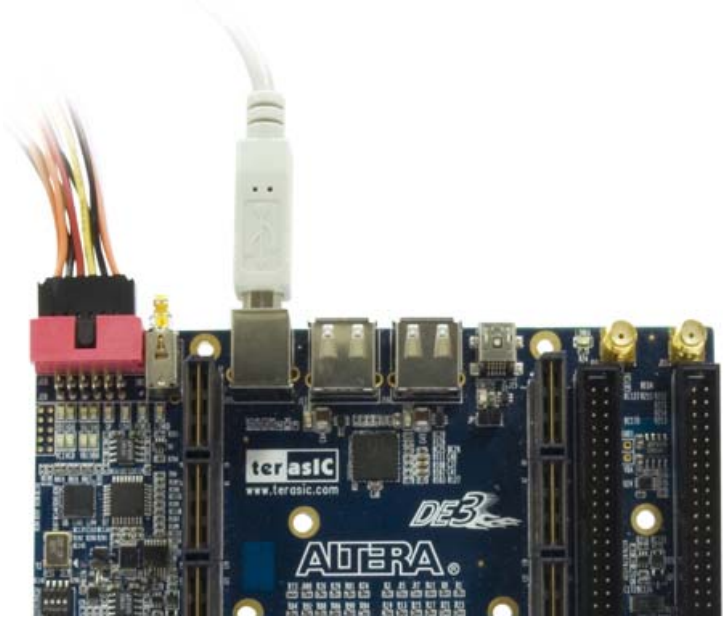


Figure 3.1. Setup of USB-Blaster cable and power cord

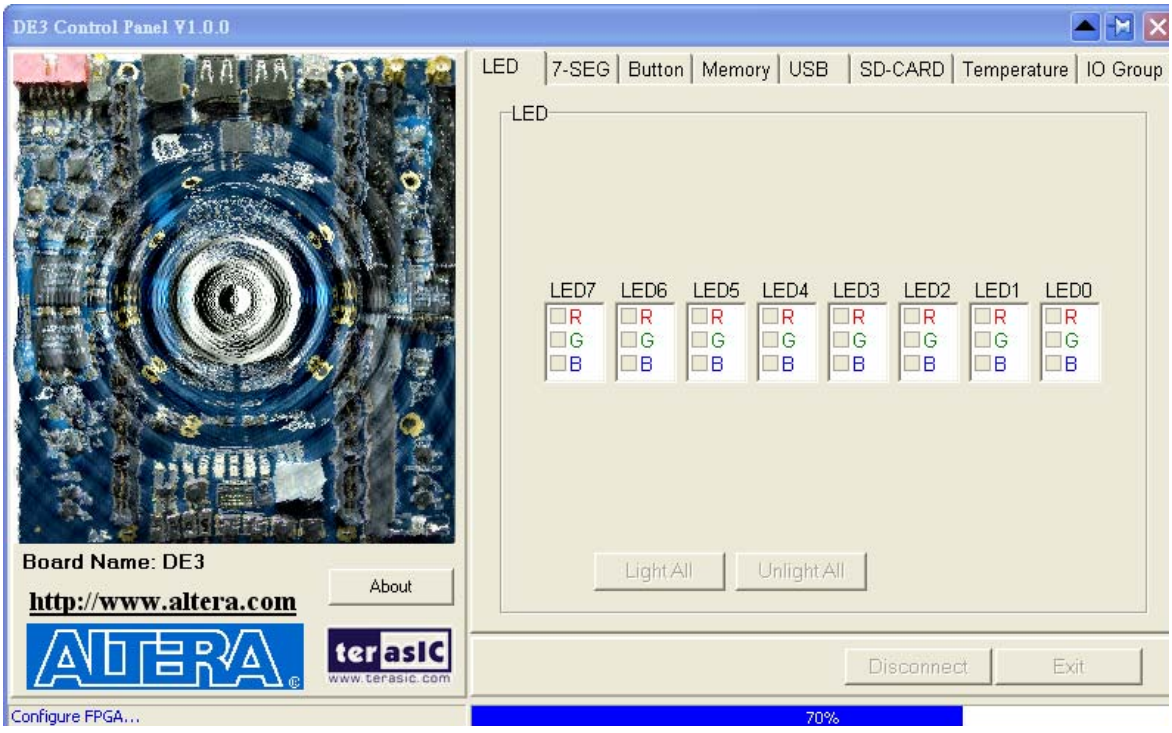


Figure 3.2. Download .sof and .elf files to the DE3 board

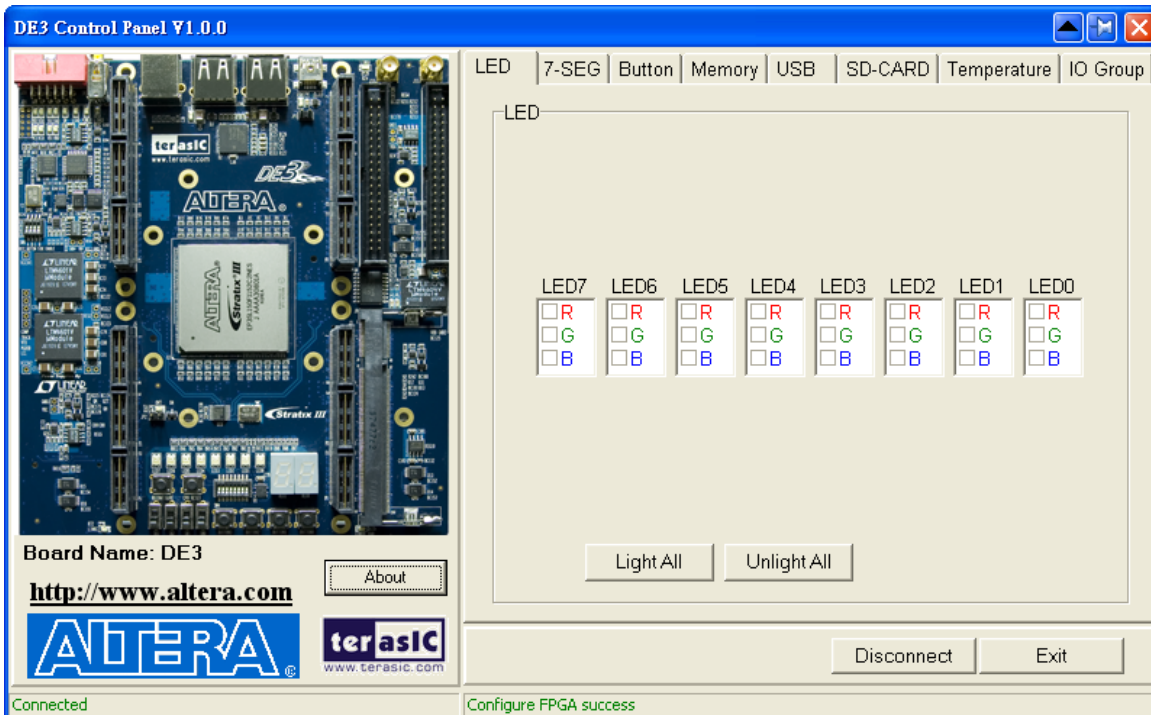


Figure 3.3. DE3 Control Panel is ready

If the connection between DE3 board and USB-Blaster is not established, or the DE3 board is not powered on before running the DE3_control_panel.exe, the Control Panel will fail to detect the FPGA and a warning message window will pop up as shown in Figure 3.4.

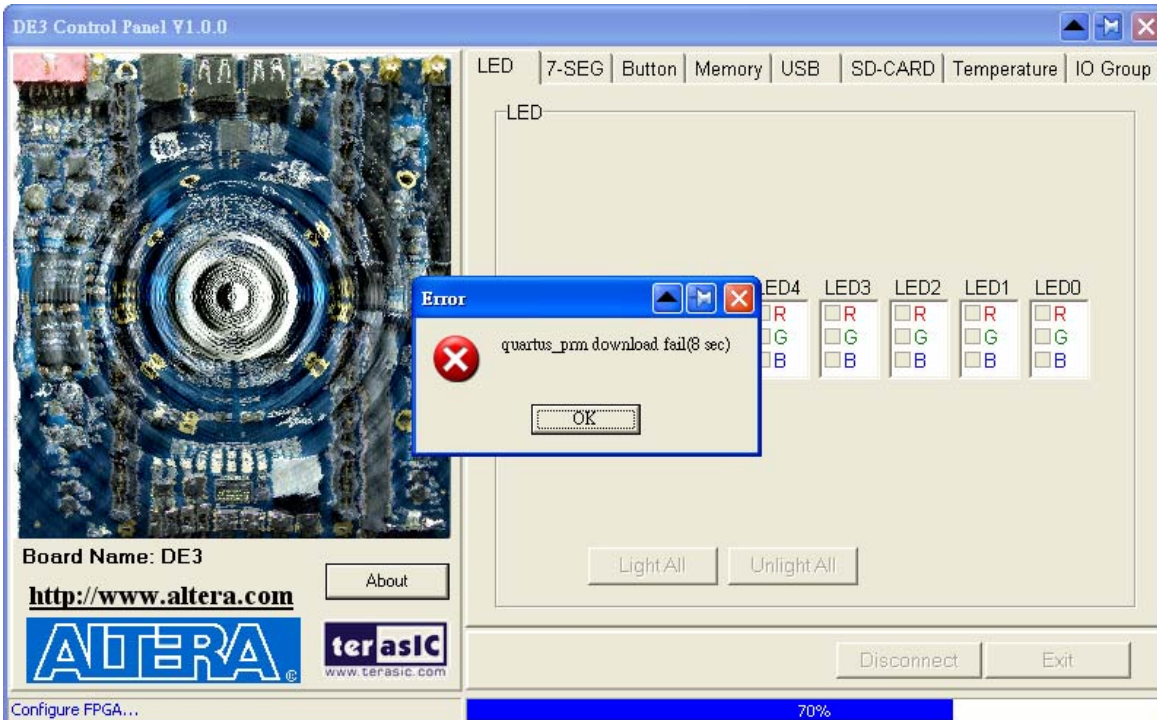


Figure 3.4. The DE3 Control Panel fails to download .sof file

The concept of the DE3 Control Panel is illustrated in Figure 3.5.The "Control Codes" which performs the control functions is implemented in the FPGA board. It communicates with the Control Panel window, which is active on the host computer, via the USB Blaster link. The graphical users interface is used to issue commands to the control codes. It handles all requests and performs data transfer between the computer and the DE3 board.

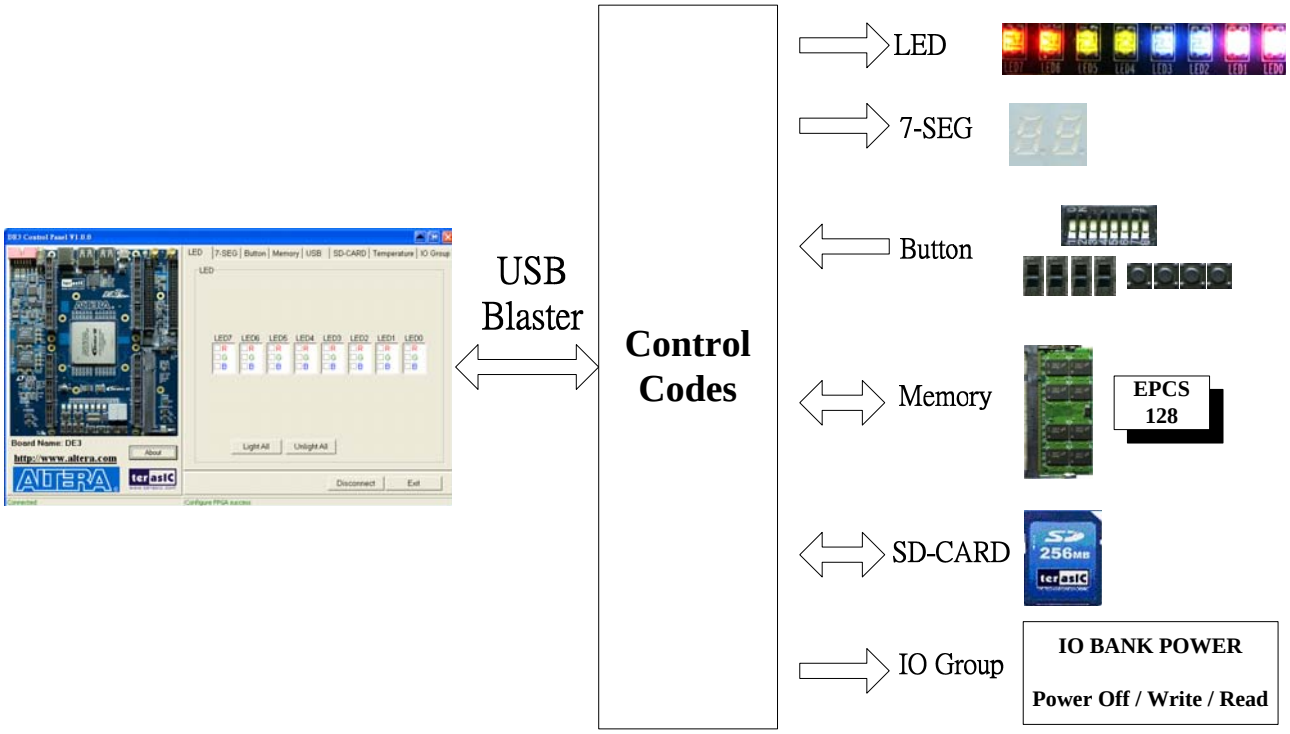


Figure 3.5. The DE3 Control Panel concept

The DE3 Control Panel can be used to light up LEDs, change the values displayed on 7-segment displays, monitoring buttons/switches status, read/write the serial configuration devices (EPCS128), access DDR2 SO-DIMM memory, read the information of SD Card, and setup the V_{CCIO} level of the I/O Groups.

3.2 Controlling the LEDs and 7-Segment Displays

One of the functions of the Control Panel is to set up the status of the LEDs and 7-segment displays. The tab-window shown in Figure 3.6 indicates where you can directly turn all the LEDs on or off individually by selecting them and clicking "Light All" or "Unlight All".

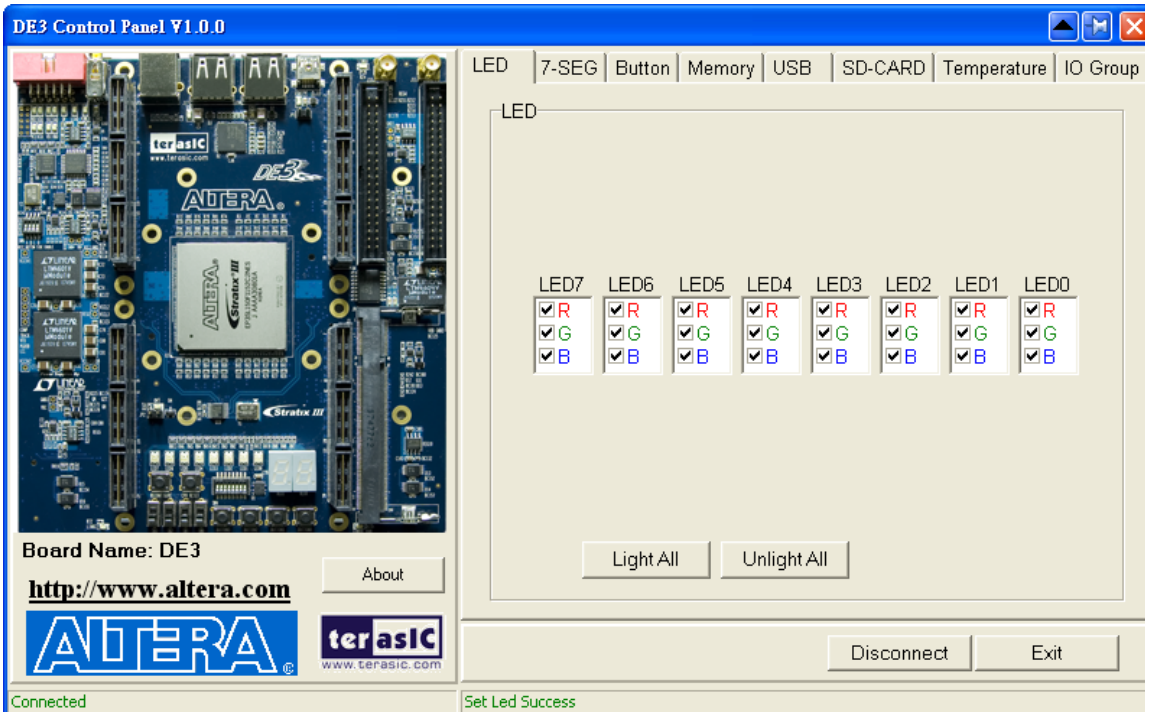


Figure 3.6. Controlling LEDs

Figure 3.7 shows the interface of the 7-SEG and how to select desired patterns. The status of the 7-SEG patterns will be updated immediately.

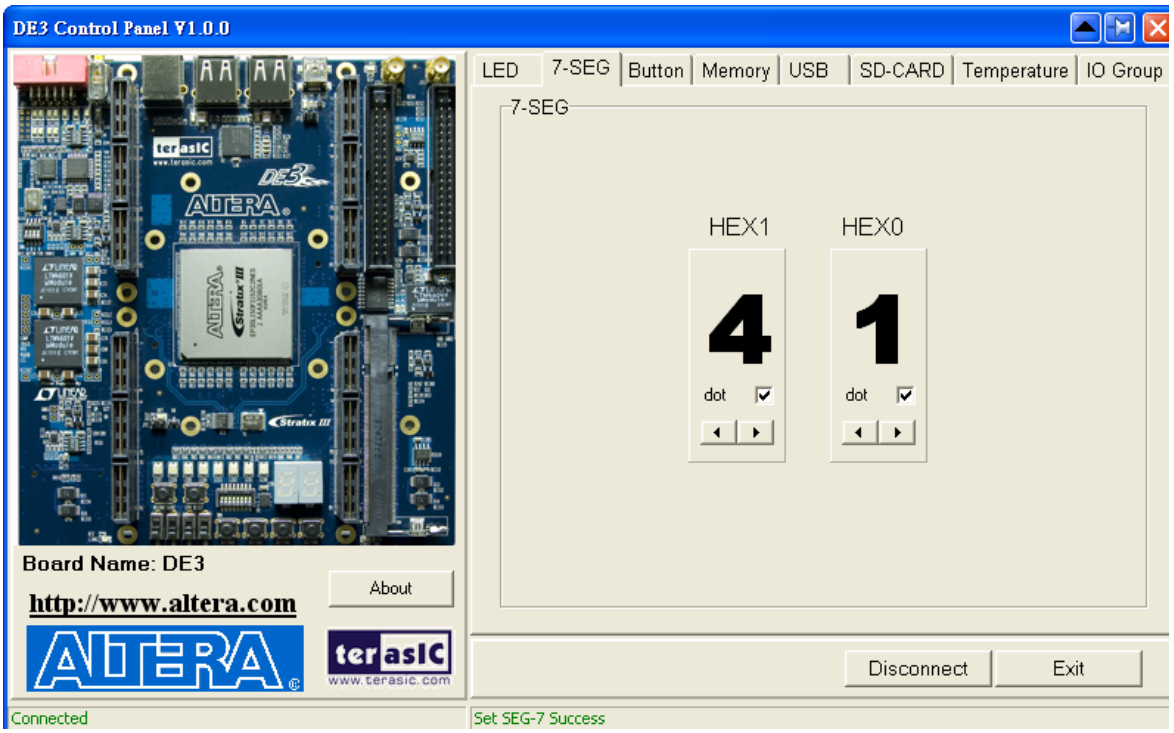


Figure 3.7. Controlling 7-SEG display

3.3 SWITCH/BUTTON

Choose the **Button** tab as shown in Figure 3.8. This function is designed to monitor status of switches and buttons from a graphic interface in real-time. It can be used to verify the functionality of switches and buttons.

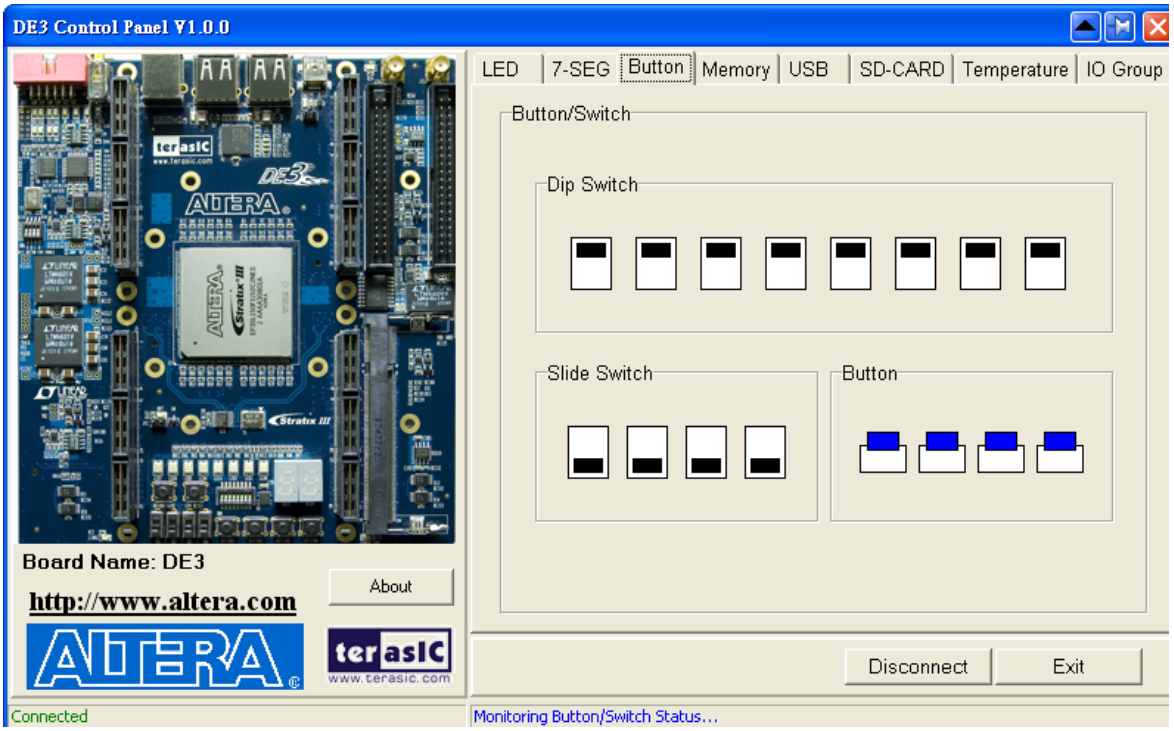


Figure 3.8. Monitoring Switches and Buttons

3.4 Memory Controller

The Control Panel can be used to write/read data to/from the DDR2 SO-DIMM memory on the DE3 board. We will describe how the DDR2 SO-DIMM is accessed. Click on the Memory tab to reach the tab-window shown in Figure 3.9.

A 16-bit string can be written into the DDR2 SO-DIMM memory by three steps, namely specifying the address of the desired location, entering the data to be written, and pressing the **Write** button. Contents of the location can be read by pressing the **Read** button. Figure 3.10 depicts the result of writing the hexadecimal value 7EFF to location 0x100, followed by reading the same location.

The Sequential Write function of the Control Panel is used to write the contents of a file to the serial configuration device, as described below:

1. Specify the starting address in the **Address** box.

2. Specify the number of bytes to be written in the **Length** box. If the entire file is to be loaded, a check mark can be placed in the **File Length** box instead of giving the number of bytes.
3. To initiate the writing of data, click on the **Write a File to Memory** button.
4. When the Control Panel responds with the standard Windows dialog box asking for the source file, specify the desired file in the usual manner.

The Sequential Read function is used to read the contents of the serial configuration device and place them into a file as follows:

1. Specify the starting address in the **Address** box.
2. Specify the number of bytes to be copied into a file in the **Length** box. If the entire contents of the serial configuration device are to be copied, then place a check mark in the **Entire Memory** box.
3. Press **Load Memory Content to a File** button.
4. When the Control Panel responds with the standard Windows dialog box ask for the destination file, users can specify the desired file in the usual manner.

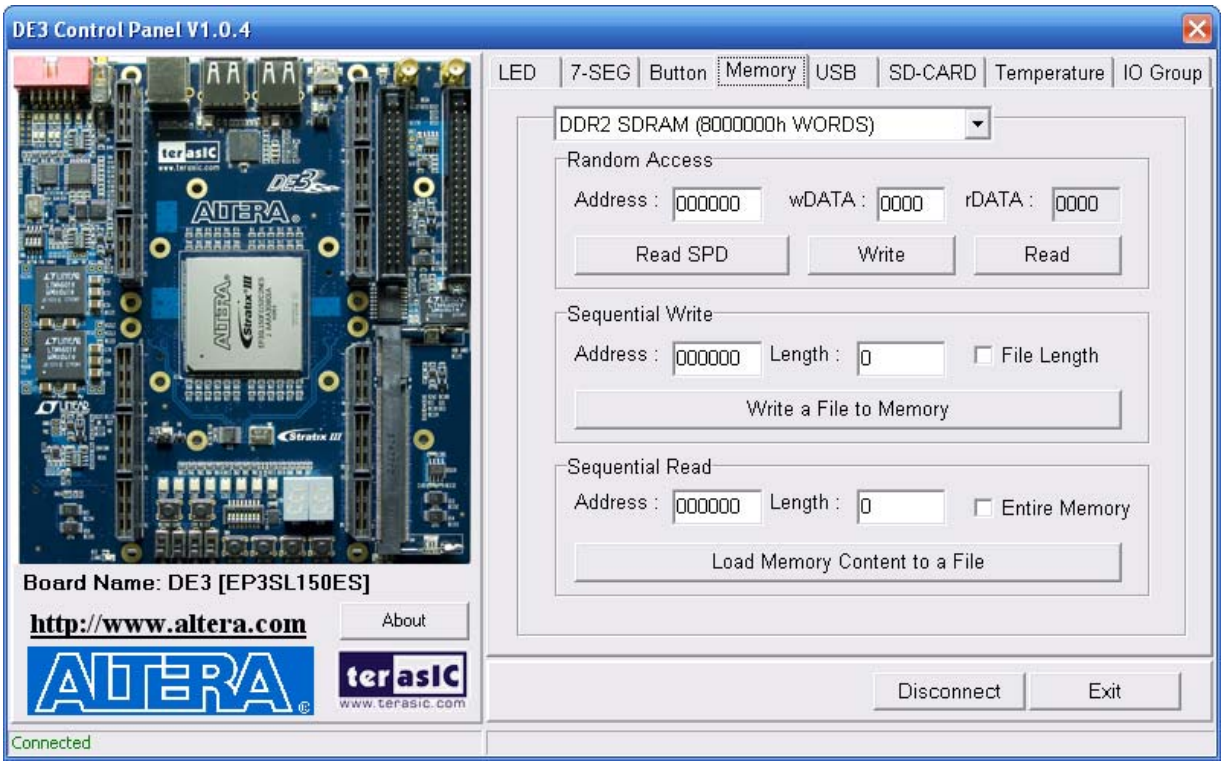


Figure 3.9. Access DDR2 SO-DIMM memory

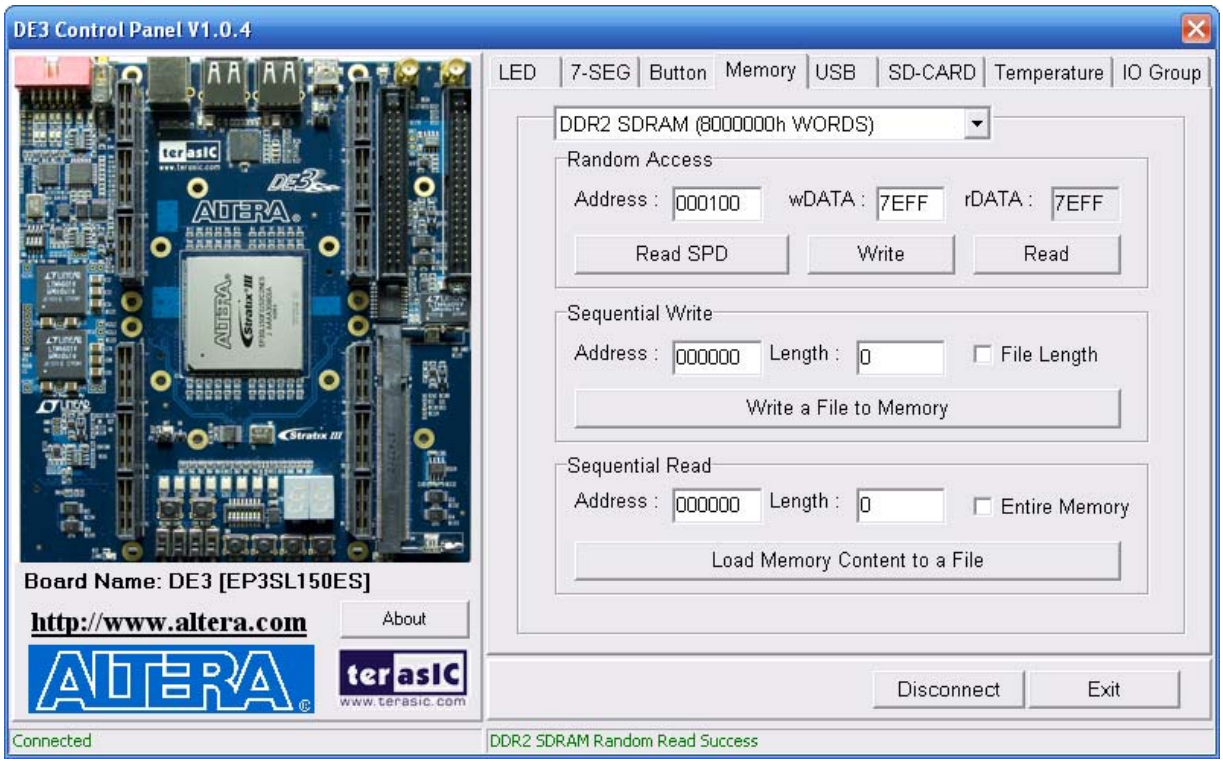


Figure 3.10. Writing the hexadecimal value 7EFF to location 0x100

3.5 USB2.0 OTG

Choose the **USB** tab to reach the window in Figure 3.11. The function is designed to monitor the status of USB Hub in real-time.

Plug a USB device to any USB port of FPGA board, and both the device type and speed will be displayed on the control window. Figure 3.11 shows a low-speed HID USB Mouse is plugged into port 3.

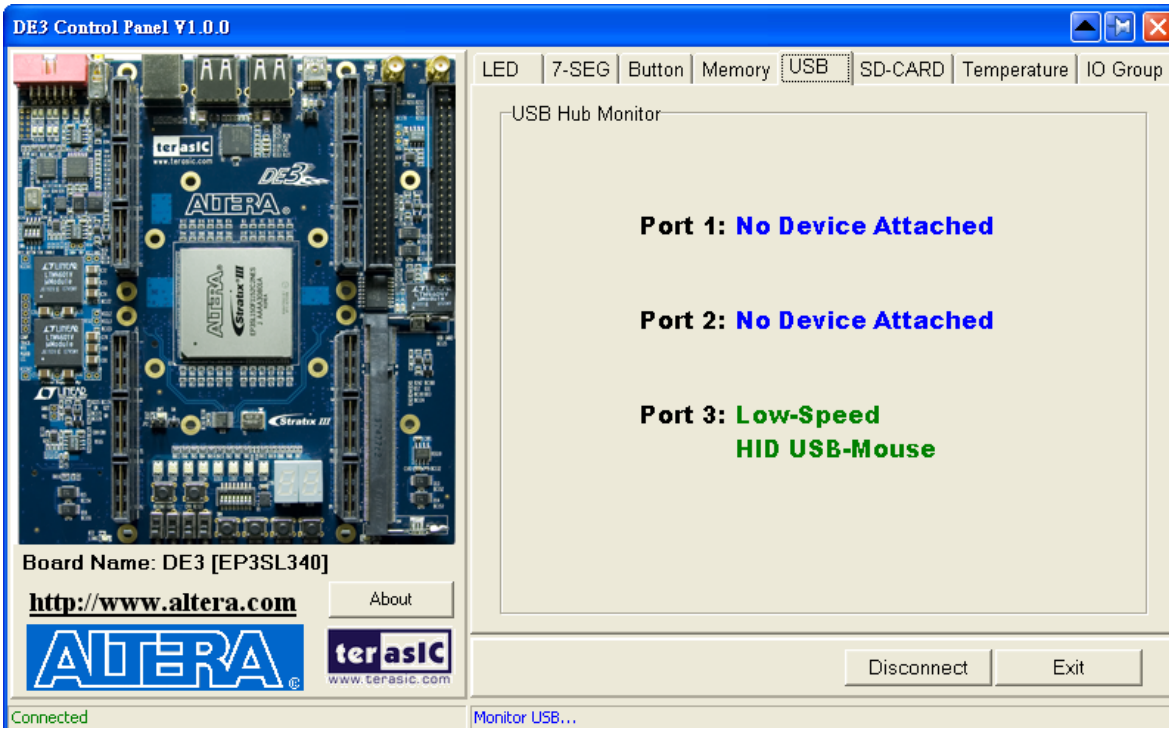


Figure 3.11. Monitoring status of USB ports

3.6 SD CARD

Choose the **SD-CARD** tab to the window shown in Figure 3.12. The function is designed to read the identification and specification of SD Card. Single-bit SD-MODE is used to access the SD Card. This function can be used to verify the functionality of SD-CARD interface.

To gather the information, simply insert a SD Card to the FPGA board and press the **Read** button. The SD-CARD identification and specification will be displayed on the control window

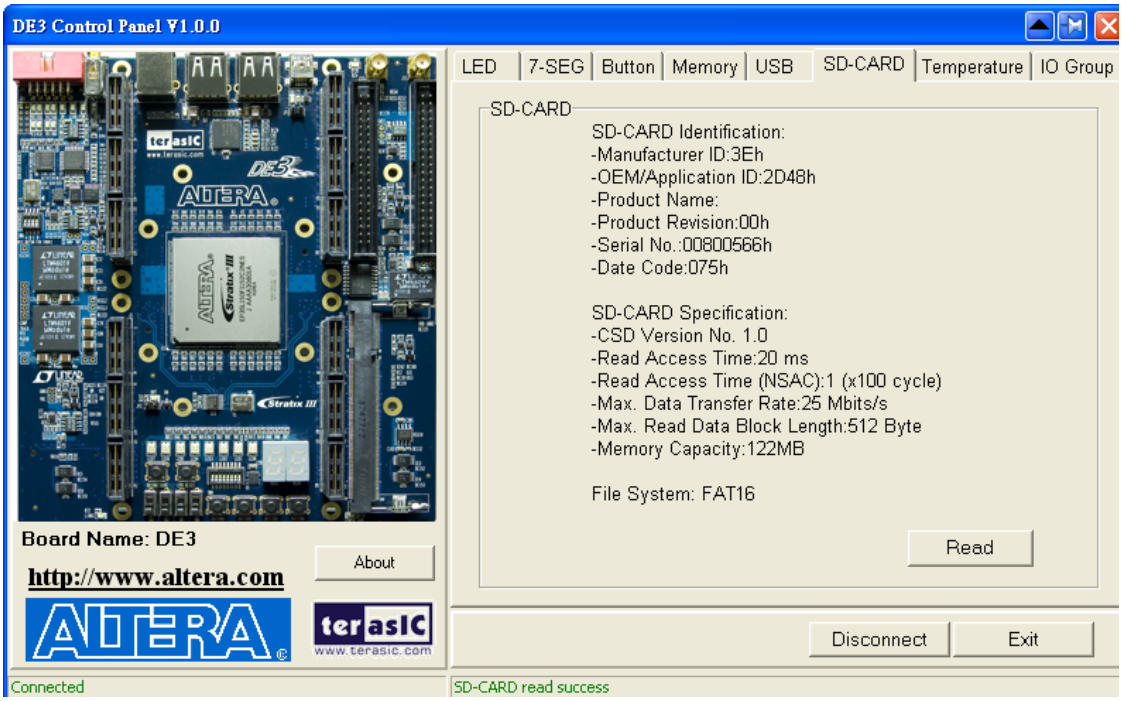


Figure 3.12. Reading the SD Card Identification and Specification

3.7 Temperature Monitor

Choose the **Temperature** tab to reach the window shown in Figure 3.13. The function is designed to control temperature sensor through Control Panel. The temperatures of Stratix III and DE3 board are shown on the right-hand side of the Control Panel.

When the temperature of Stratix III exceeds the Maximum setting of Over Temperature or Alert, a warning message will be shown on the Control Panel. Click “Read” button to get current settings for Over temperature and Alert. Users can enter the maximum and minimum temperatures for Over temperature or Alert as required. Click the “Write” button to update the values entered.

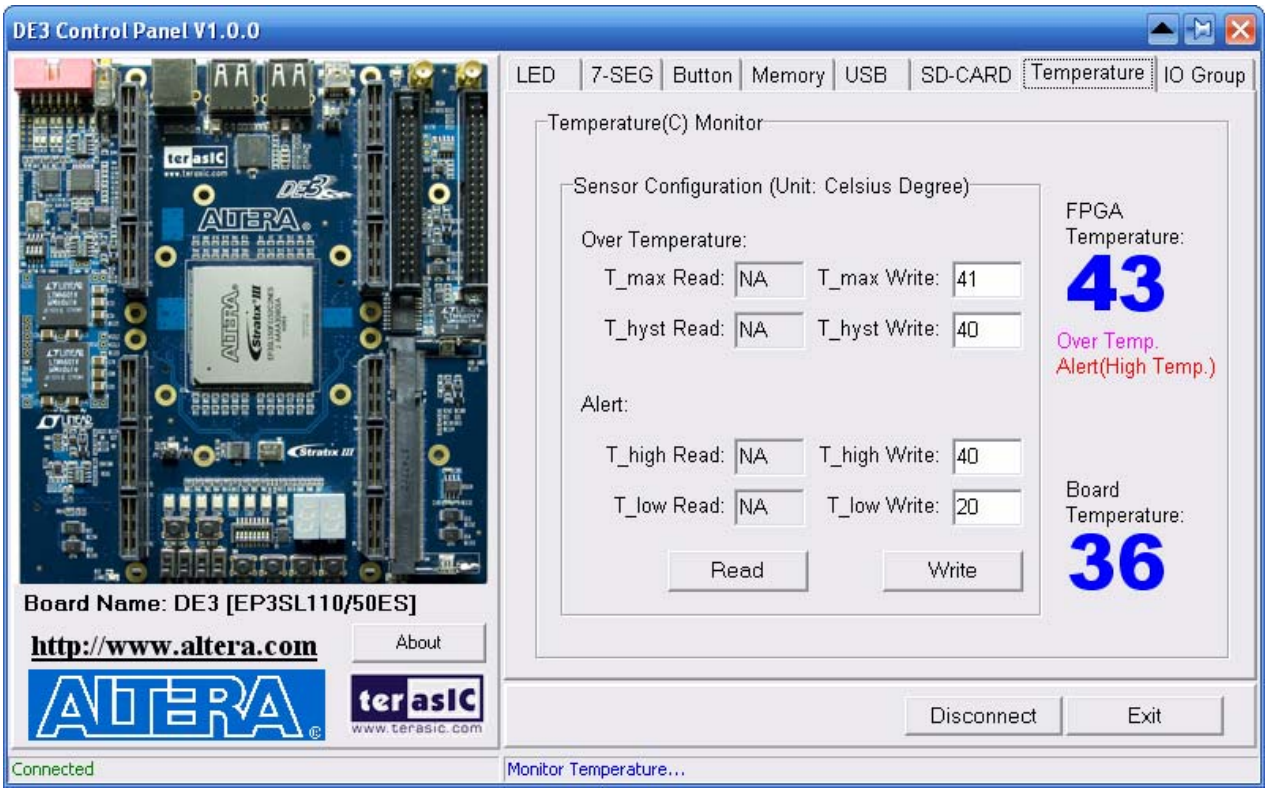


Figure 3.13. Accessing the Temperature Sensor through Control Panel

3.8 I/O Group

Choose the **I/O Group** tab to reach the window shown in Figure 3.14. The function is designed to read/write and control the V_{CCIO} level of all I/O Groups of the DE3 board.

Click the “Read” button to enter the window shown in Figure 3.15. Current V_{CCIO} level of all I/O Groups will be displayed.

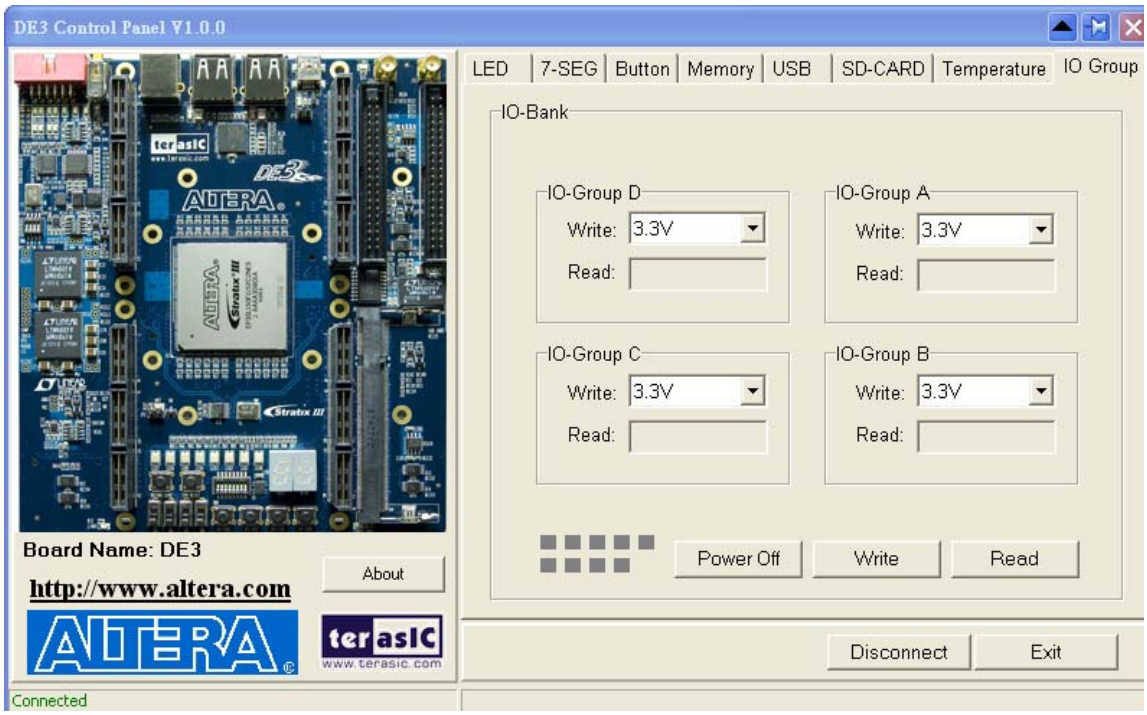


Figure 3.14. Accessing the power status of all I/O Groups

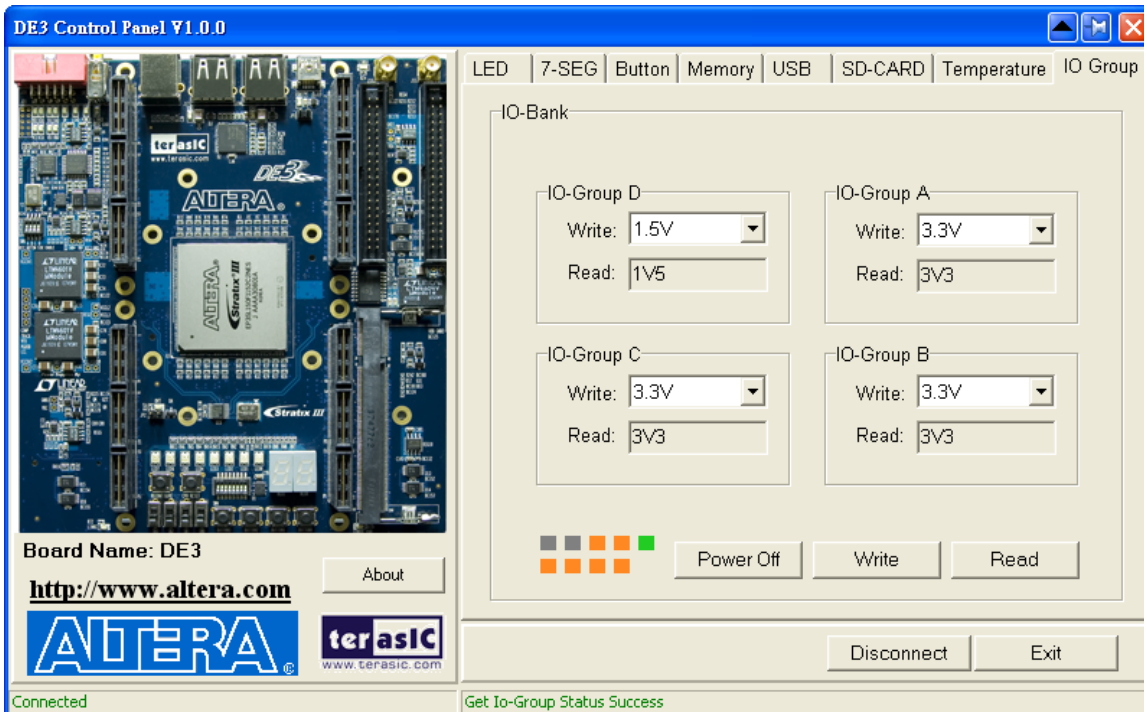


Figure 3.15. Reading the V_{CCIO} level of all I/O Groups

3.9 Overall Structure of the DE3 Control Panel

The DE3 Control Panel communicates with control codes, which are instantiated in the Stratix III FPGA..

To run the Control Panel, users must set it up first, as explained in Section 3.1. Figure 3.16 depicts the structure of the Control Panel. Each input/output device is controlled by the NIOS II Processor instantiated in the FPGA chip. The communication with the PC is done via the USB Blaster link. The NIOS II interprets the commands sent from the PC and performs the appropriate actions.

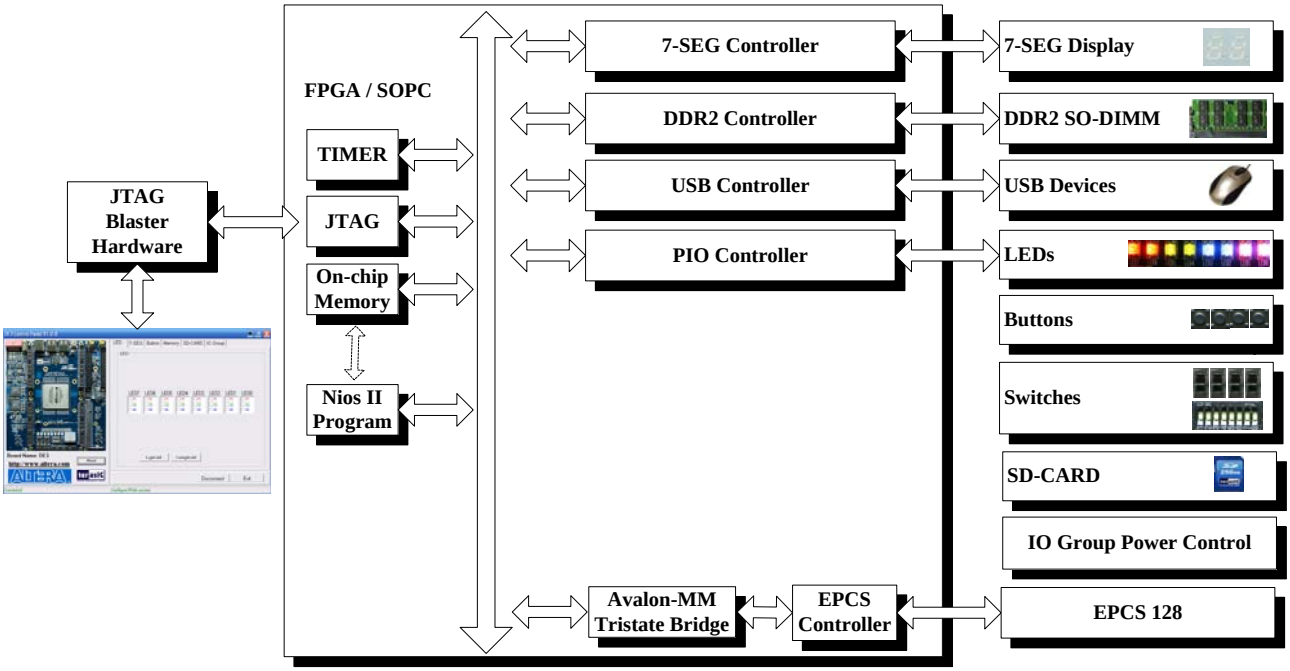


Figure 3.16. The block diagram of the DE3 control panel

Chapter 4
DE3 System Builder

This chapter describes how to create a custom design project on the DE3 board by using DE3 System Builder.

4.1 Introduction

The **DE3 System Builder** is designed to assist users to create a Quartus II project for DE3 board within minutes. The generated Quartus II project files include:

- Quartus II Project File (.qpf)
- Quartus II Setting File (.qsf)
- Top-Level Deign File (.v)
- Synopsis Design Constraints file (.sdc)
- Encrypted Power Configuration Controller (.v)
- Pin Assignment Document (.htm)

The DE3 System Builder not only can generate the files above, but also can provide error-checking rules to prevent users from making the following common mistakes:

1. Board damaged for wrong pin/bank voltage assignment.
2. Board malfunction caused by wrong device connections or missing pin counts for connected ends.
3. Performance dropped because of improper pin assignments.

4.2 General Design Flow

This section will introduce the general design flow to build a project for the DE3 board via the DE3 System Builder. The general design flow is illustrated in the Figure 4.1.

First of all, users should launch DE3 System Builder and create a new project according to the requirement. When users complete the settings, the DE3 System Builder will generate three major files, which include top-level deign file (.v), encrypted power configuration controller (.v), and Quartus II setting file (.qsf).

The top-level deign file contains top-level verilog wrapper for users to add their own design/logic. The encrypted power configuration controller file contains encrypted core which is generated by user's selection on I/O Group voltage. The Quartus II setting file contains information such as FPGA device type, top-level pin assignment, and I/O standard for each user-defined I/O pin.

Next, users must be aware that they can never modify encrypted power configuration controller file. User's own design should be included within top-level deign file.

Finally, Quartus II programmer must be used to download SOF file to DE3 board using JTAG interface.

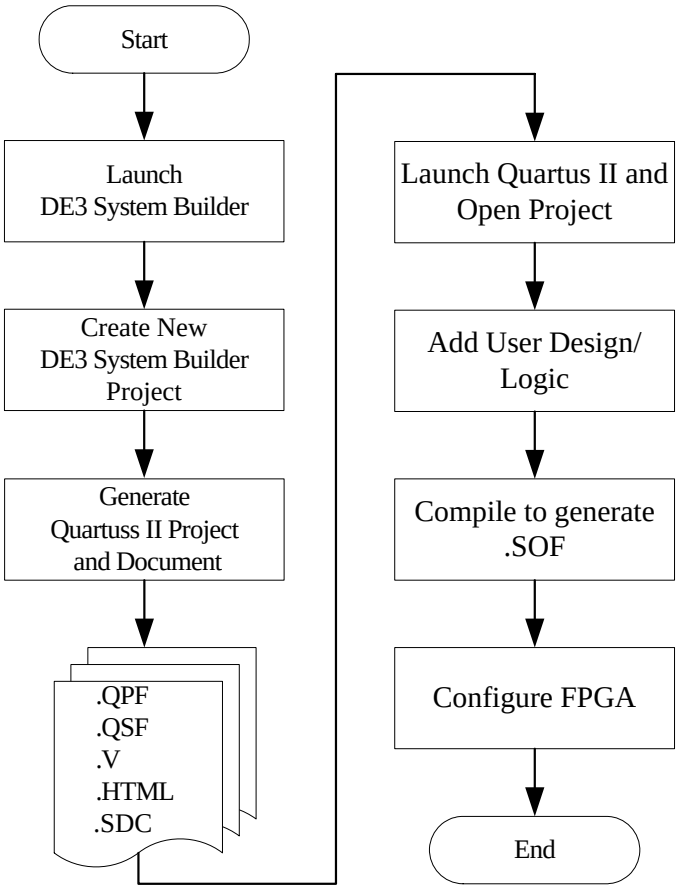


Figure 4.1. The general design flow of building a design
for the DE3 board via the DE3 System Builder

4.3 Using DE3 System Builder

This section provides the detail procedures on how to use the DE3 System Builder.

- **Install and active the DE3 System Builder**

  The DE3 System Builder is located in the directory: "**Tool\DE3_System_Builder**" in the DE3 System CD. Users can copy the whole folder to a host computer without installing the utility. Before using the DE3 System Builder, perform the following steps:

  - Make sure the license file of the "**Encrypted Power Configuration Controller IP"** is set in the Quartus II software. (Please refer to the section *Add the License File for Terasic Power Controller IP* in the document named "*Getting start with Altera DE3 board*" for more information on how to import a license file.)
  - Execute **DE3_System_Builder.exe** on the host computer. The DE3 System Builder user-interface will appear, as shown in Figure 4.2.

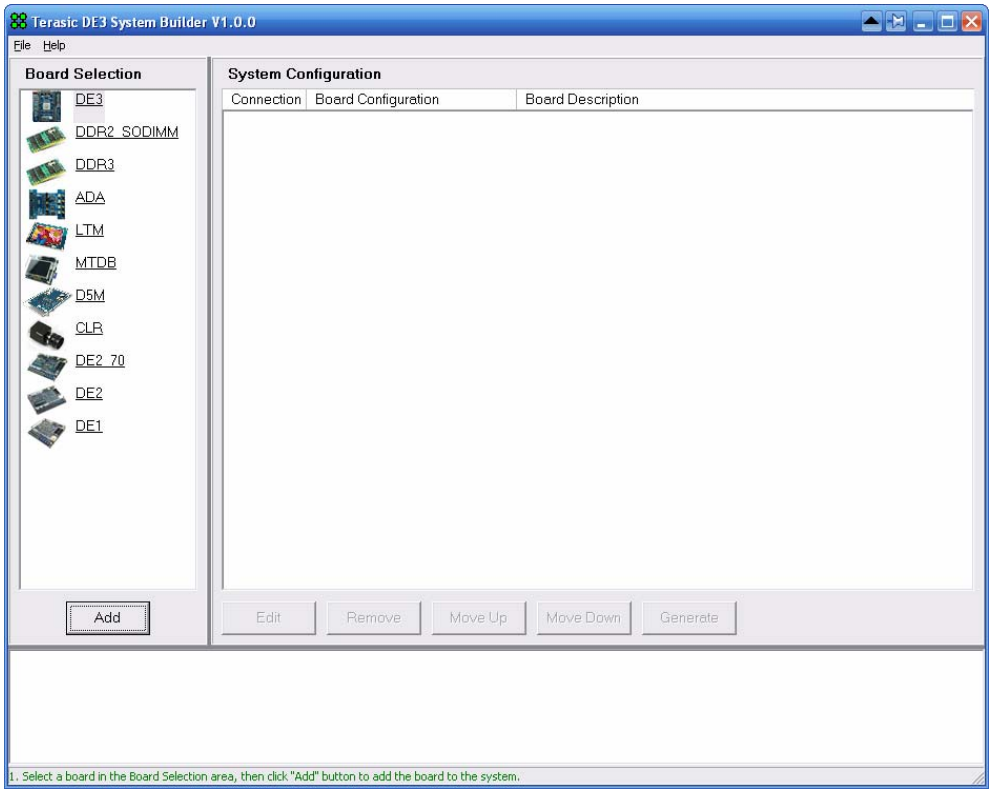


Figure 4.2. The DE3 System Builder window

- **Add Board**

  On the left-hand side of the DE3 System Builder, there are many boards' icons in the **Board Selection** field. If users select a **DE3** board and click **Add** button, a **DE3 Configuration** window will pop up. After the setting is completed, a DE3 board will be added to the **System Configuration** field.

If users select any of the daughter boards in the **Board Selection** field, a window will pop up and allow users to change the name of the daughter board. Click **OK** to add the daughter board to **System Configuration** Filed.

DE3 Configuration

When users add a DE3 board, a **DE3 Configuration** window will pop up as shown in Figure 4.3. This window allows users to configure many features for the DE3 board as described below:

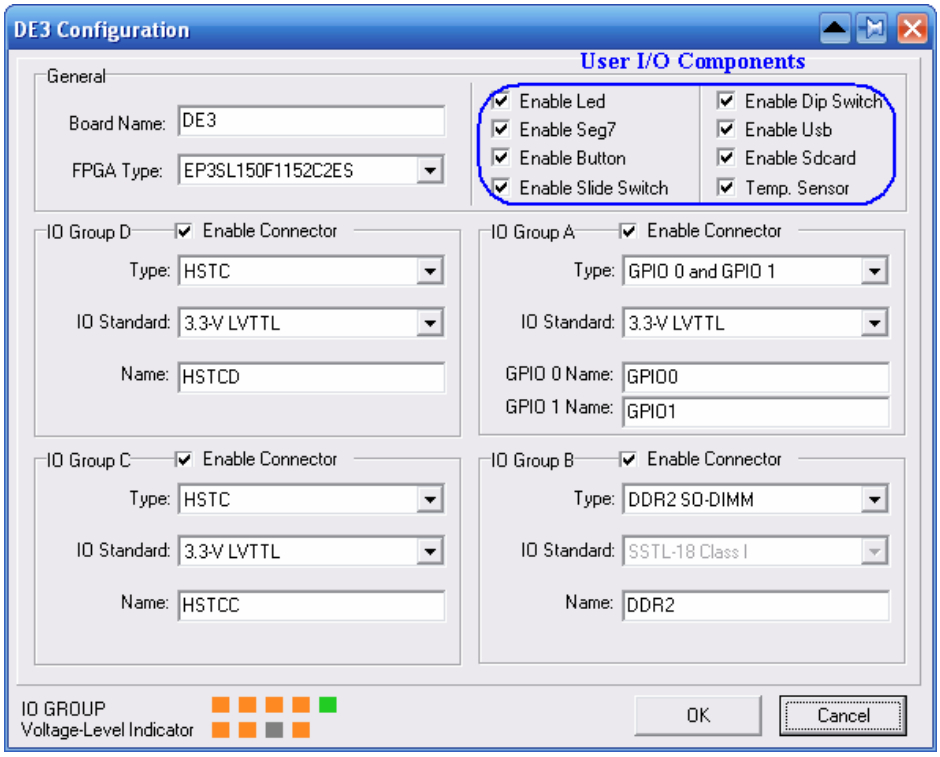


Figure 4.3. The DE3 Configuration window

- **Board Name:** The board name will be set as the Quartus II project name when it is created by DE3 System Builder.

- **FPGA Type**: The FPGA device on DE3 board may be EP3SL150 or EP3SH340. Users need to select the FPGA device and speed grade accordingly.

- **User I/O Components:** Users can enable or disable the User I/O Component from this field. If the User I/O component is enabled, the DE3 System Builder will generate the port name, port connection rules (input/output) and the pin assignments for the User I/O component on the Quartus II top-level file.

- **IO Group:** There are four I/O Groups in the DE3 Configuration window. The HSTC connector A, B, C, and D correspond to I/O Groups A, B, C, and D on DE3 board, respectively. Disabled I/O Groups will not be listed in the Quartus II top-level file. There are three options for each I/O Group as listed below:

    i. **Type:** Users can select a connector type for I/O Group A and B**.,** as the HSTC connector A and B share the same I/O bus with the GPIO expansion headers and DDRII SO-DIMM socket.
    ii. **I/O standard:** Users can select the I/O standard for the I/O Group.
    iii. **Name:** Users can change the name of a connector.

- **I/O GROUP Voltage-level Indicator:** This function will indicate the V_{CCIO} level for current I/O standard setting of the four I/O Croups. The status is same as the LEDs on the DE3 board. Please refer to Section 2.4 for details.

Connection Between Two Connectors

When users add a DE3 board and daughter board in the System configuration field, it is necessary to establish the connection in between. The port name, port connection rules (input/output) and the pin assignment of the connector in the top-level file will be fully compatible with this daughter board. The detailed steps for the connection setup are shown below:

- **Establish and remove a connection between two connectors:**

    i. Move the mouse cursor to the upper connector as shown in Figure 4.4.

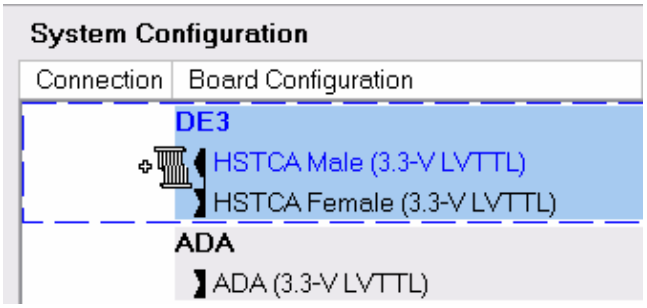


Figure 4.4. Step 1 of establishing a connection.

    ii. Hold the left button of the mouse and Drag the mouse cursor to the lower connector as shown in Figure 4.5.

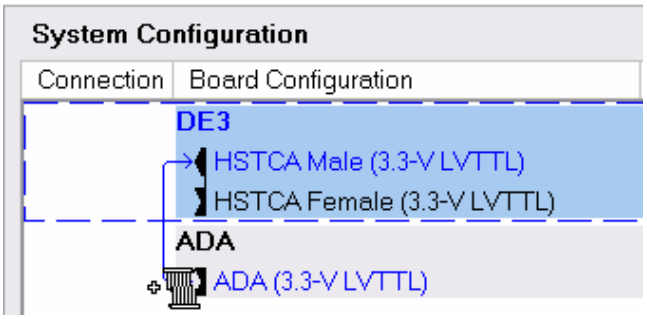


Figure 4.5. Step 2 of establishing a connection

iii. Release the left mouse button and a green connection line will be drawn between two connectors as shown in Figure 4.6.

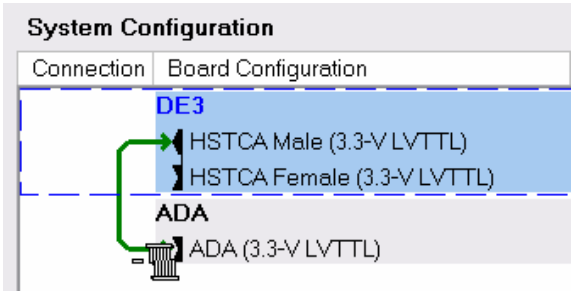


Figure 4.6. Step 3 of establishing a connection

iv. Redo the steps i to iii will remove an established connection as shown in Figure 4.7.

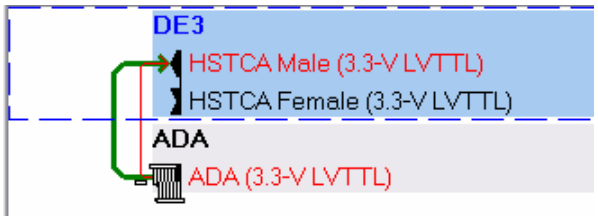


Figure 4.7. The step for removing a connection between two connectors

- **Warning message of an incorrect connection**
  If users try to establish a connection between two different types and I/O standard of connectors, a warning message box will pop up as shown in Figure 4.8.

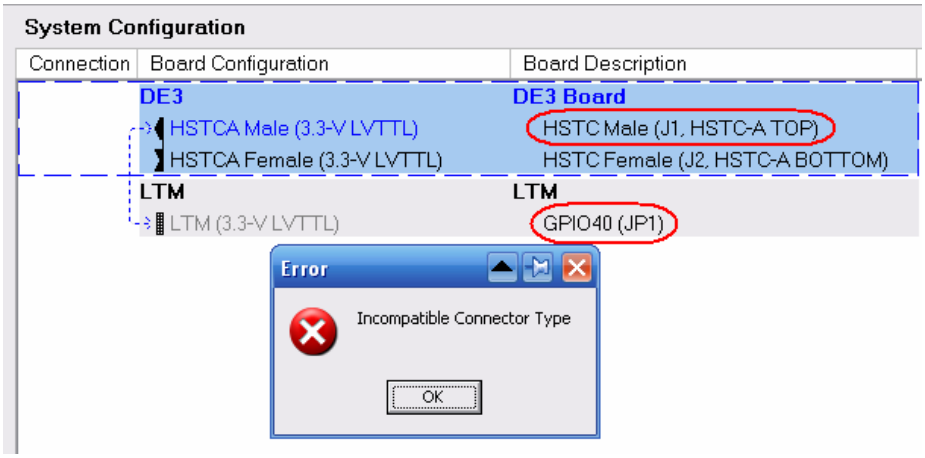


Figure 4.8. The error message box of an incorrect connection

■ **Project Generation**

When users press the **Generate** button, the DE3 System Builder will generate the corresponding Quartus II files and documents as listed in the Table 4-1:

Table 4-1. The files generated by DE3 System Builder

No.	Filename	Description
1	<Board name>.v	Top level verilog file for Quartus II
2	IOV_<IO Group voltage level>.v	Encrypted Power Configuration Controller IP
3	<Board name>.qpf	Quartus II Project File
4	<Board name>.qsf	Quartus II Setting File
5	<Board name>.sdc	Synopsis Design Constraints file for Quartus II
6	<Board name>.htm	Pin Assignment Document

Users can use Quartus II software to add custom logic into the project and compile the project to generate the SRAM Object File (.sof).

In addition, the Encrypted Power Configuration Controller IP is used to control the V_{CCIO} level of the I/O Groups. This IP file is included in the Quartus II top-level file as listed in below:

```
//=============================================
//  IO Group Voltage Configuration (Do not modify it)
//=============================================
IOV_A3V3_B3V3_C3V3_D3V3 IOV_Instance(
    iCLK(OSC2_50),
    iRST_n(1'b1),
    iENABLE(1'b0),
    oREADY(),
    oERR(),
    oERRCODE(),
    oJVC_CLK(JVC_CLK),
    oJVC_CS(JVC_CS),
    oJVC_DATAOUT(JVC_DATAOUT),
    iJVC_DATAIN(JVC_DATAIN)
);
```

Users should never modify this module. The filename of this IP varies from the VCCIO level of the I/O Group. For example, the filename IOV_A3V3_B1V8_C3V3_D2V5.v means that the VCCIO voltage level of the I/O Group A, B, C, and D are 3.3V, 1.8V, 3.3V, and 2.5V, respectively.

■ **Project Open/Close/Save/Save As**

The DE3 System also provides functions to open, close, and save user's system configuration file. Users can save the current system configuration information into a .scf file and load it to the DE3 System Builder. All these functions can be found in the **File** menu as indicated in Figure 4.9.

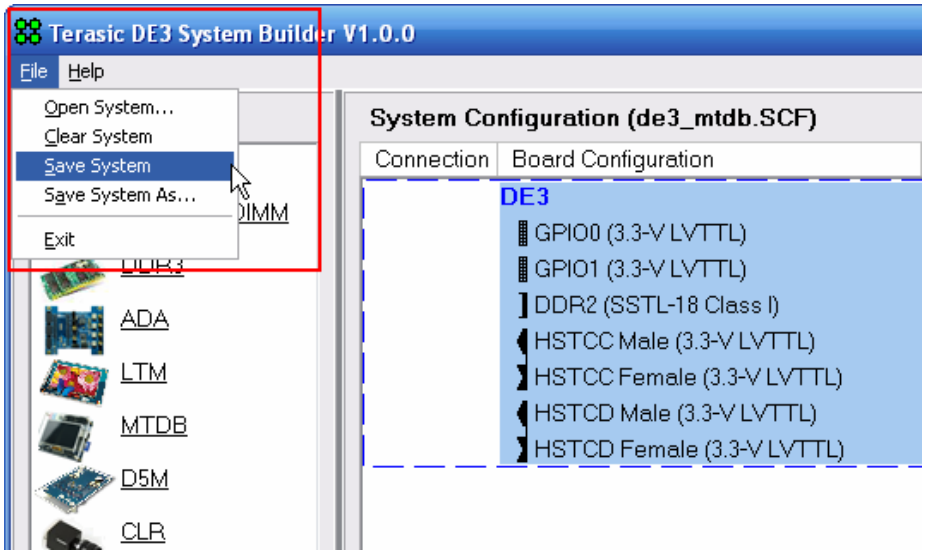


Figure 4.9. The File menu of the DE3 System Builder

4.4 Creating My First DE3 Project

This section provides an example on how to generate a Quartus II project to turn on LEDs of the DE3 board via the DE3 System Builder. The detail procedures are described below:

1. Execute *DE3_System_Builder.exe* on the host computer.

2. **Add a DE3 board :**
   Select a **DE3** board's icon in the **Board Selection** field and click **Add** button.

3. **Configure the DE3 I/O interface:**
   After the above is completed, a **DE3 Configuration** window will pop up. Please follow Figure 4.10 to modify the configuration as described below:
   i. Change the **Board Name** from **DE3** to **MY_FISRT_DE3_PROJECT**.
   ii. Make sure the **FPGA type** is same as user's DE3 board.
   iii. Disable all the components and IO Group except the **LED.**
   iv. Click **OK** button to complete the configuration.

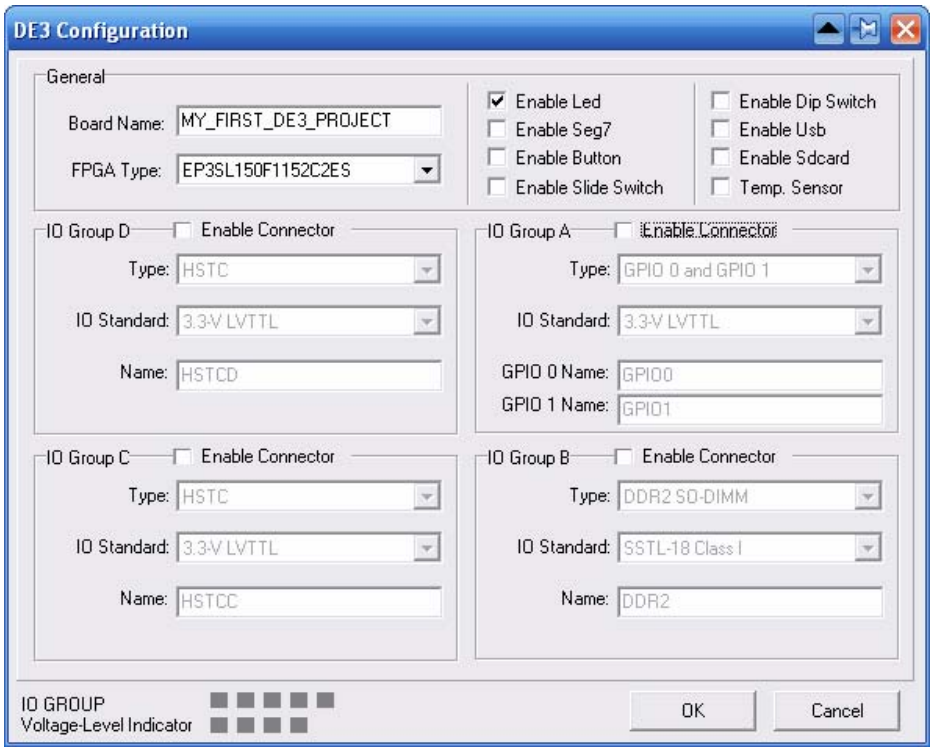


Figure 4.10. The DE3 Configuration window

4. **Complete the project:**
   Click **Generate** to complete this project. The DE3 System Builder will generate the corresponding Quartus II project files under the directory specified by users.

5. **Add user logic design:**
   i. Use Quartus II software to open the project generated.
   ii. Open the top level file **MY_FIRST_DE3_PROJECT.v** and add the following user logic:

```
//=======================================
//  Structural coding
//=======================================
assign LEDR = 8'hff; // Turn OFF the LEDR0~LEDR7
assign LEDG = 8'hff; // Turn OFF the LEDG0~LEDG7
assign LEDB = 8'h00; // Turn ON  the LEDB0~LEDB7
```

   iii. Compile the project to generate the SRAM Object files (.sof)

6. **Configure the FPGA device:**
   i. Before configuring the FPGA device on the DE3 board, please make sure all the boards are removed from the DE3 board.
   ii. Configure the FPGA device via the USB cable.
   iii. Check the LED status of the I/O GROUP Voltage-level Indicator. The LEDs should be turned off because all I/O groups are disabled.
   Finally, check the status of the LED0~LED7 on the DE3 board. The LEDs should be lightening in blue.

4.5 Connect TERASIC Daughter Boards to a DE3 Board

This section describes how to create a project when connecting a DE3 board with a Terasic daughter board via the DE3 System Builder. The DE3 System Builder will provide the following features:

- The I/O standard and the pin names of the HSTC connector pins will be fully compatible with Terasic daughter board.
- The DE3 System Builder will select the correct V_{CCIO} voltage level of the I/O Group for users automatically.

An example of connecting a Terasic Multimedia Touch Panel Daughter Board (MTDB) with DE3 board as shown in Figure 4.11 will be demonstrated. Detailed procedures are listed below:

1. **Executable *DE3_System_Builder.exe* on the host computer.**

2. **Add a DE3 board.**

3. **Configure the DE3 I/O interface:**
   Please refer to the Figure 4.12 to modify the related configuration as described below:

i. Change the **Board Name** from **DE3** to **DE3_MTDB**.

ii. Make sure the **FPGA type** is same as user's DE3 board.

iii. Disable all the components and IO Group except for **IO Group C.**

iv. Click **OK** button to complete the configuration.

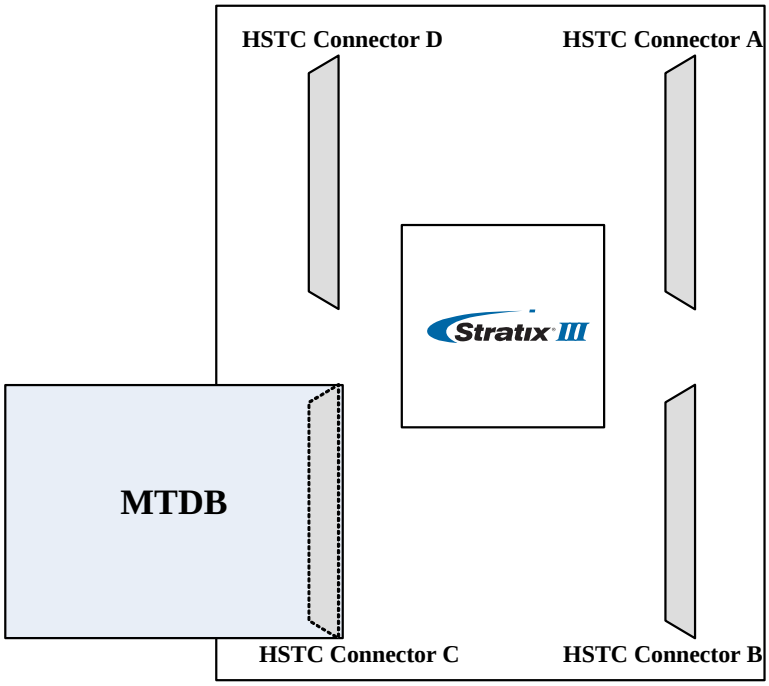


Figure 4.11 The hardware connection for the demonstration

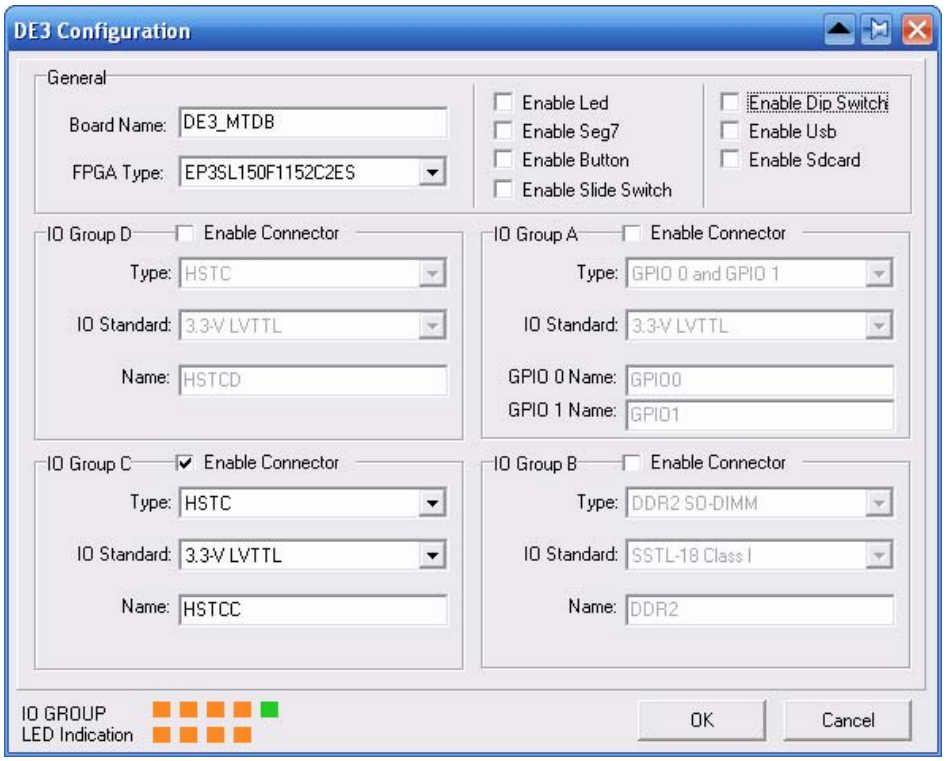


Figure 4.12. The Configuration for the example

4. **Add a Terasic daughter board:**
   i. Select a **MTDB** board from the **Board Selection** field and click **Add** button.
   ii. A window will pop up and allows users to change the name of the daughter board. Click **OK** to add the daughter to the system configuration field. Figure 4.13 shows the DE3 board and MTDB board are in the system configuration field..

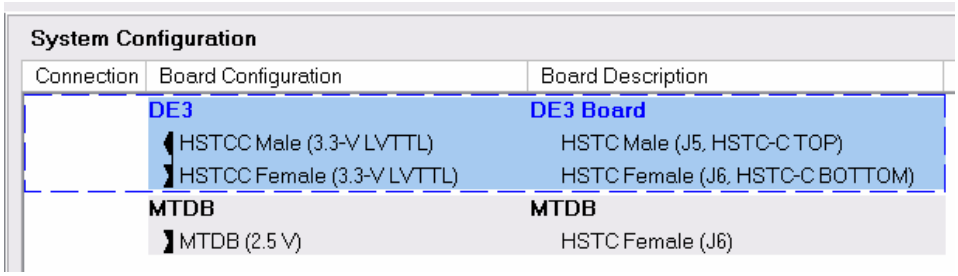


Figure 4.13. The System Configuration field of the DE3 System Builder

5. **Establish a connection between DE3 board and MTDB board:**
   i. In the **System Configuration** field, establish a connection from the **HSTCC Male** connector of the DE3 board and the MTDB board shown in Figure 4.14.

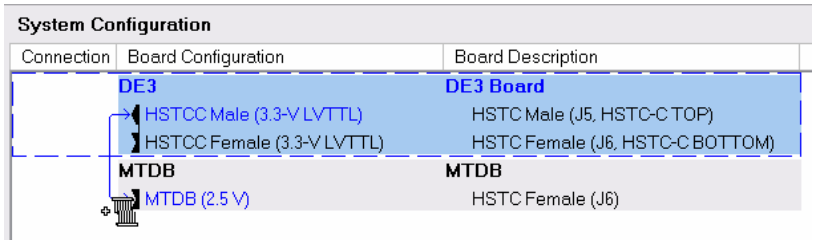


Figure 4.14. Establish a connection between the DE3 board and the MTDB board

   ii. After the connection is established, the DE3 System Builder will change the I/O standard of the connector to fit with the daughter board automatically as shown in Figure 4.15. The I/O standard of the **HSTCC male** connector has been changed from 3.3-V LVTTL to 2.5V.

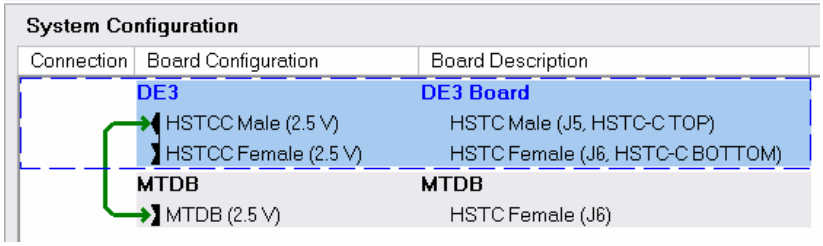


Figure 4.15. The connection between DE3 board and MTDB board

6. **Complete the project:**
   Click **Generate** to complete this project.

7. **Add custom design:**
   i. Use Quartus II software to open the project created previously.
   ii. Open the top-level file **DE3_MTDB.v,** users can find that the DE3 System Builder has created the I/O port name, I/O direction and pin assignments for the MTDB board:

```
////////// HSTCC (J5 HSTC-C TOP/J6, HSTC-C BOTTOM), connect to
MTDB(MTDB Board) //////////
output                      HSTCC_ADC_DCLK;
input                       HSTCC_TX_CLK;
output                      HSTCC_ADC_DIN;
input                       HSTCC_ADC_PENIRQ_n;
output     [7:0]            HSTCC_LCD_DATA;
.
.
.
```

   iii. Users can add the user logic into the project to access the MTDB board.
   iv. Compile the project to generate the SRAM Object files (.sof)

8. **Configure the FPGA device:**
   i. If the generated project is configured to FPGA device for the first time, please make sure all the boards are removed from the DE3 board before powering up.
   ii. Configure the FPGA device via the USB cable.
   iii. Check the status of I/O Group indication LEDs to see if the voltage level for I/O Group is correct.
   iv. Power off the DE3 board and plug the MTDB board to the HSTC connector C (J5) onboard.
   v. Configure the FPGA device via the USB cable again and check the user logic function for MTDB board.

4.6 Connect Multiple DE3 Boards

This section provides a demonstration on how to create a project when two DE3 boards are connected via the DE3 System Builder. Figure 4.16 shows the connection for the two DE3 boards. Detailed procedures are listed below:

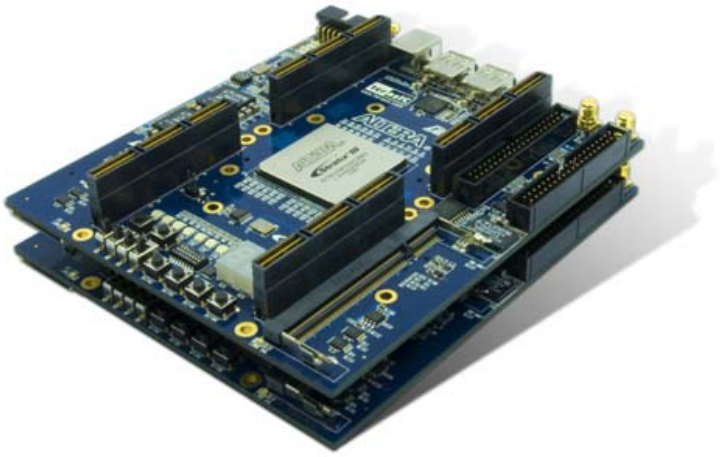


Figure 4.16. The connection of two DE3 boards

1. **Executable *DE3_System_Builder.exe* on the host computer.**

2. **Add a DE3.**

3. **Configure the DE3 I/O interface:**
   Please refer to the Figure 4.17 to modify the associated configuration as described below:
   i. Change the **Board Name** from **DE3** to **DE3_TOP**.
   ii. Make sure the **FPGA Type** is the same as user's DE3 board.
   iii. Click **OK** button to complete the configuration.

4. **Add another DE3 board into system:**
   i. Repeat the step2 to step3 to add another DE3 board.
   ii. Change the **Board Name** from **DE3** to **DE3_BOTTOM**.
   iii. Change all the type of I/O Groups to **HSTC.**
   iv. Make sure the I/O standard of all I/O Groups is same as the other DE3 board.

5. **Establish connections between two DE3 boards:**
   In the **System Configuration** field, established connection between two DE3 boards is shown in Figure 4.18.

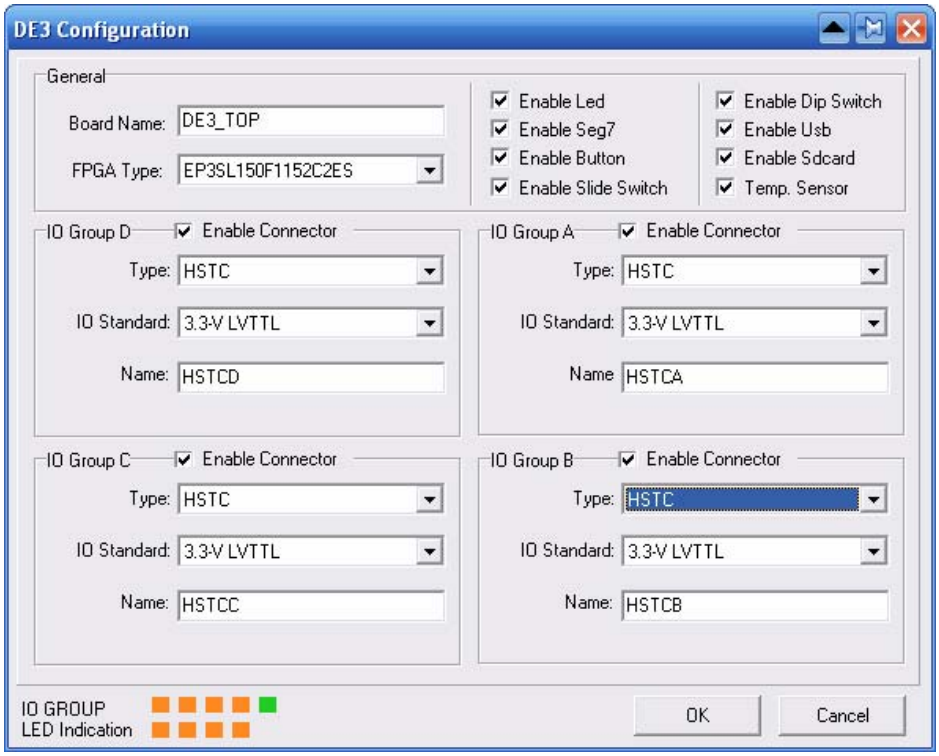


Figure 4.17. The DE3 Configuration window

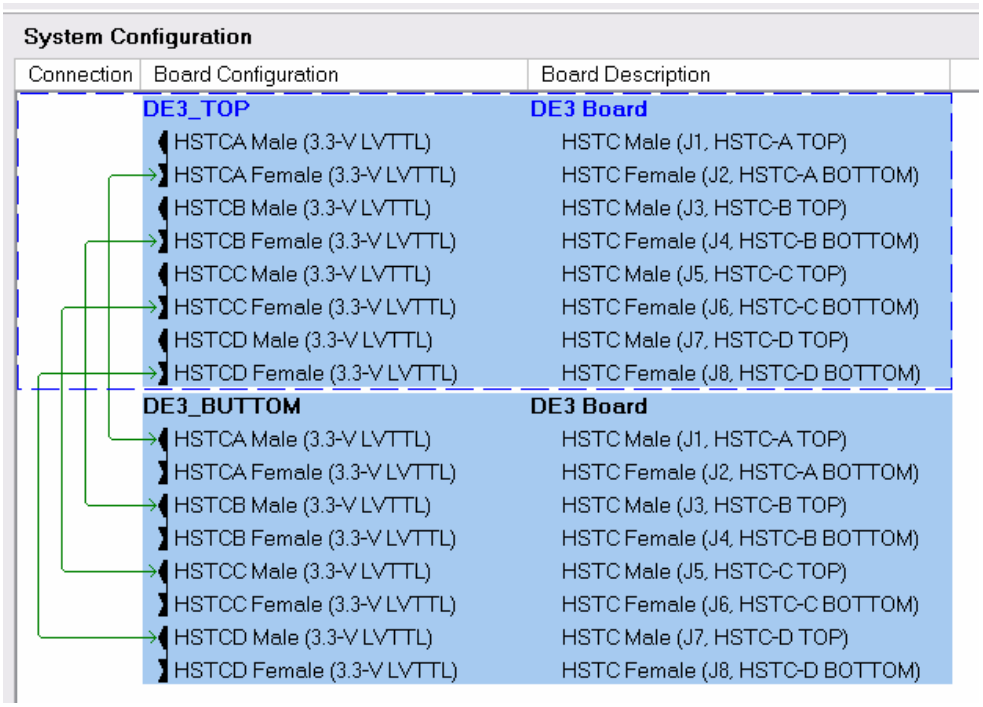


Figure 4.18. The connection between the two DE3 boards

6. **Complete the project:**
   Click **Generate** to complete this project, and the DE3 System Builder will generate **two** Quartus II projects named **DE3_TOP** and **DE3_BOTTOM**.

7. **Add custom design:**
   i. The DE3_System_Builder will generate the HSTC connector port name and set the I/O direction to bi-directional in the top-level file:

```
////////// HSTCA (J1, HSTC-A TOP/J2, HSTC-A BOTTOM), connect to DE3
//////////
inout      [129:0]         HSTCA_IO;
inout                      HSTCA_SDA;
output                     HSTCA_SCL;

////////// HSTCB (J3, HSTC-B TOP/J4, HSTC-B BOTTOM), connect to DE3
//////////
inout      [129:0]         HSTCB_IO;
inout                      HSTCB_SDA;
output                     HSTCB_SCL;
.
.
.
```

   ii. User can include user logic design to the top-level file and compile the project to generate the SOF file.

8. **Configure the FPGA device**

4.7 Connect a Custom-Made Daughter Board to the DE3 Board

If users want to connect a custom-made daughter board to the DE3 board, the most important thing is to make sure that both DE3 board and the custom daughter board support the same I/O standard. The following example shows how to connect a custom daughter board with 3.3V I/O standard to the GPIO connector of the DE3 board.

1. **Executable *DE3_System_Builder.exe* on the host computer.**

2. **Add a DE3 board.**

3. **Configure the DE3 I/O interface:**
   Please refer to the Figure 4.19 to modify the associated configuration as described below:
   i. Change the **Board Name** from **DE3** to **DE3_CUSTOM_DESIGN**.
   ii. Make sure the **FPGA type** is the same as user's DE3 board.

iii. Disable all the I/O Groups except for I/O Group A**.**

iv. Click **OK** button to complete the configuration.

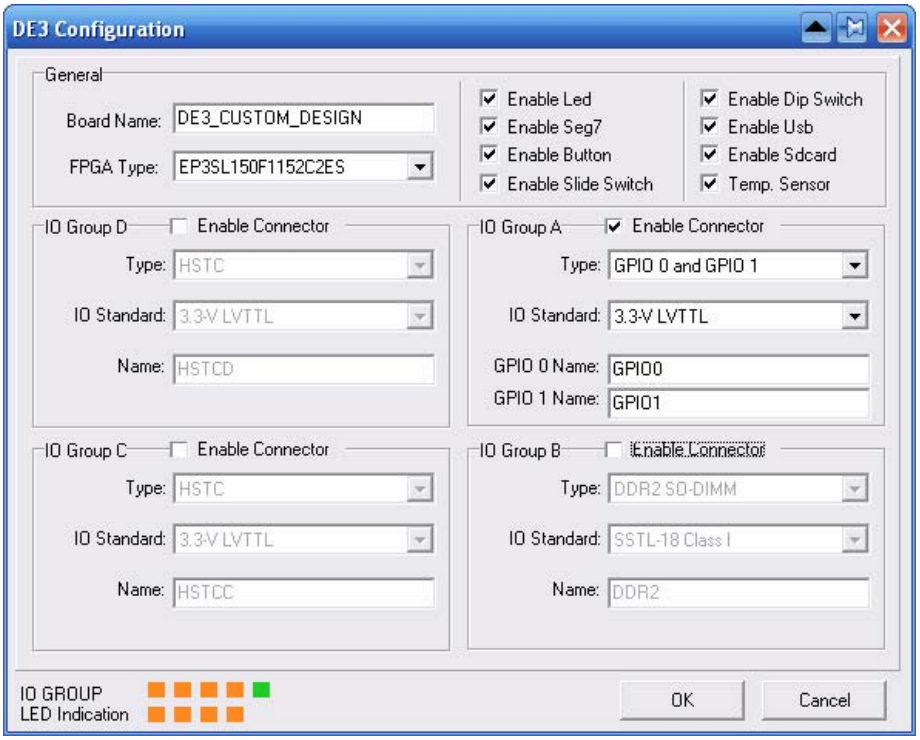


Figure 4.19. The DE3 Configuration window

4. **Complete the project:**

Click **Generate** to complete this project.

5. **Add custom logic design:**

i. Users can include their own logic design to the top-level file generated by DE3 System Builder and compile the project to generate the SRAM object files (.sof).

6. **Configure the FPGA device:**

i. If the generated project is configured to FPGA device for the first time, please make sure all the boards are removed from the DE3 board before powering up.

ii. Configure the FPGA device via the USB cable.

iii. Check the status of I/O Group indication LEDs to see if the voltage level of I/O Group is correct.

iv. Power off the DE3 board and plug the custom-made board to the GPIO 0(J14) of the DE3 board.

v. Configure the FPGA device via the USB cable again and check the user logic function for the custom-made board.

Chapter 5
Examples of Advanced Demonstration

This chapter provides a number of examples of advanced circuits implemented on the DE3 board. These circuits demonstrate the major features onboard, such as its SD card, USB host and device, and DDR2. For each demonstration the Stratix III FPGA configuration file is provided, as well as full source code in Verilog HDL code. All of the associated files can be found in the *DE3_demonstrations* folder from the **DE3 System CD**. There are four sub-folders named 340, 260, 150ES, and 150 under the directory of DE3_demonstrations. The numbers correspond to the Stratix III FPGA EP3SL340, EP3E260, EP3S150ES, and EP3S150 on DE3 board. For each of demonstrations described in the following sections, we give the name of the project directory for its files, which are sub-directories of the *DE3_demonstrations* folder.

5.1 USB Host

USB is a well-known communication standard used in many peripherals. The DE3 board provides a complete USB solution for both host and device applications. In this demonstration, USB host functions are implemented for USB mass-storage and Human-interface devices (HIDs) USB-Mouse. The drivers of the above applications are implemented in NIOS II C code. All high-speed, full-speed, and low-speed devices are supported in this demonstration.

Figure 5.1 shows the hardware system block diagram of this demonstration. The system requires a 50 MHz clock provided from the board. The PLL generates a 100 MHz clock for NIOS II processor and high-speed controllers, and generate 10 MHz clock for low-speed peripherals, such as buttons. A custom-defined SOPC ISP1761 controller, developed by TERASIC, is used to connect the ISP1761 USB chip and NIOS II processor. Based on this controller, NIOS II processor can access the register, memory, and interrupts of the USB chip. A PIO pin, named usb_reset_n, is connected to the USB for performing hardware reset of the USB chip. The NIOS II program is stored in the On-Chip Memory.

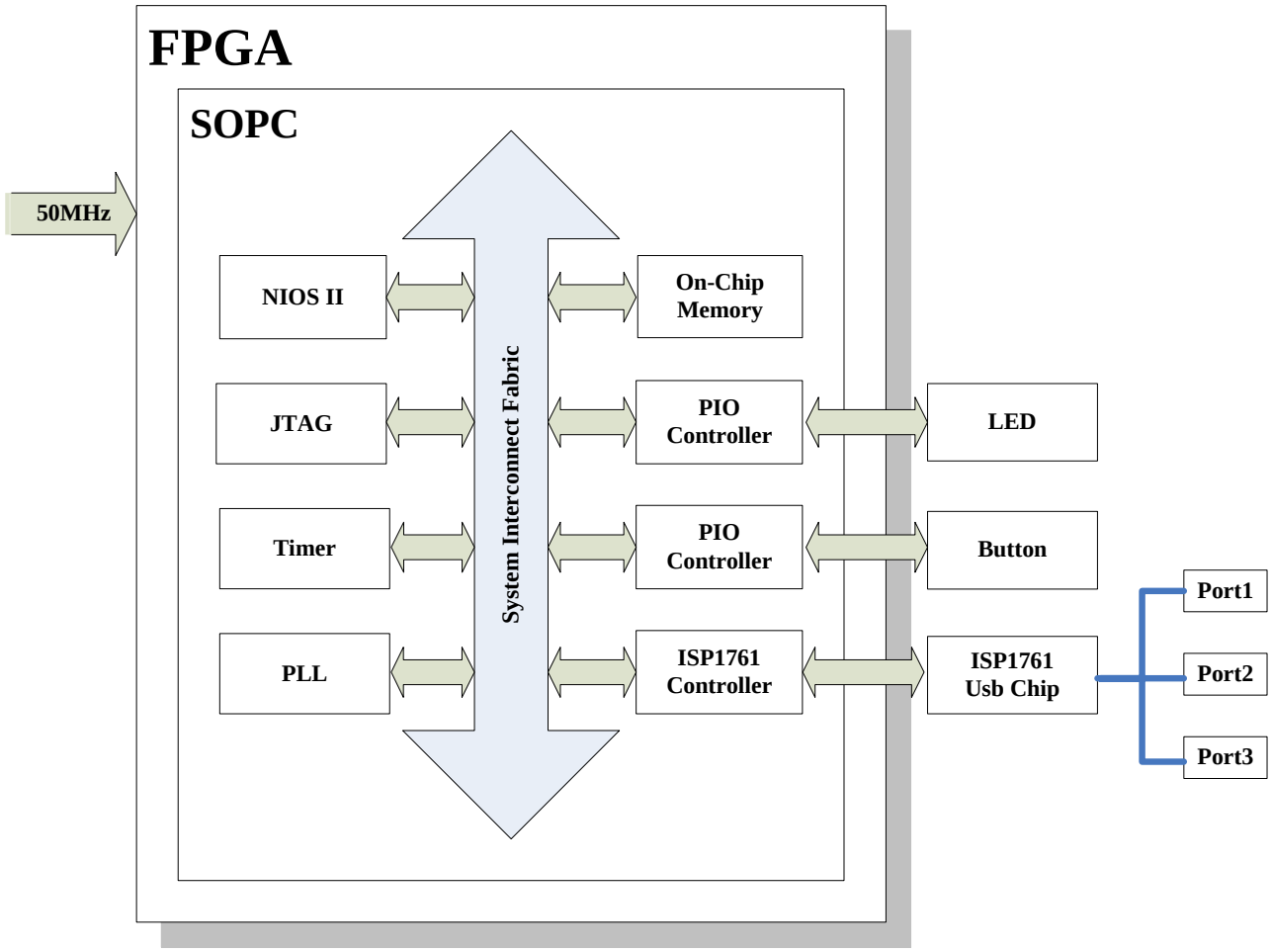


Figure 5.1. Hardware Block Diagram of the USB-Host Demonstration

Figure 5.2 shows the NIOS II software stack of this demonstration. NIOS PIO block is provided by NIOS II System. The block provides basic IO functions IORD and IOWR to access hardware directly. The function prototypes are defined in the header file <io.h>. The ISP 1761 HAL block implements functions to access internal registers and memories of the USB chip ISP 1761, and high/full/low speed transfer functions for isochronous, interrupt, control, and bulk transfers. USB Host controller block implements control functions for ISP1761 Host Controller. USB protocol block implements USB protocol, including USB-Hub protocol. The USB-Mouse Class Driver implements functions to communicate with HID USB-Mouse. The USB mass-storage Class Driver implements functions to communicate with Bulk-Only Transport USB mass-storage based on “USB Floppy Interface” (UFI) Command Set. UFI is defined based on the SCSI-2 and SFF-8070i command set. The FAT File System block implements reading functions for FAT16 and FAT 32 file system. Long filename is supported in this function block.

The workflow of the main block is shown in Figure 5.3. The standard output of this program is JTAG-URAT. In the demo batch file, the output message will be display in nios2-terminal. When the program detects an USB mass-storage device, it will list the files in root directory. If a file

named “test.txt” is found, the program will dump the file contents. When an HID USB-Mouse is detected, the program will poll the mouse status continuously and display the relative information in standard output.

In this demonstration, NIOS II uses PIO mode to access the internal memory of ISP1761. For high throughput application, DMA implementation and interrupt can enhance data transfer rate significantly.

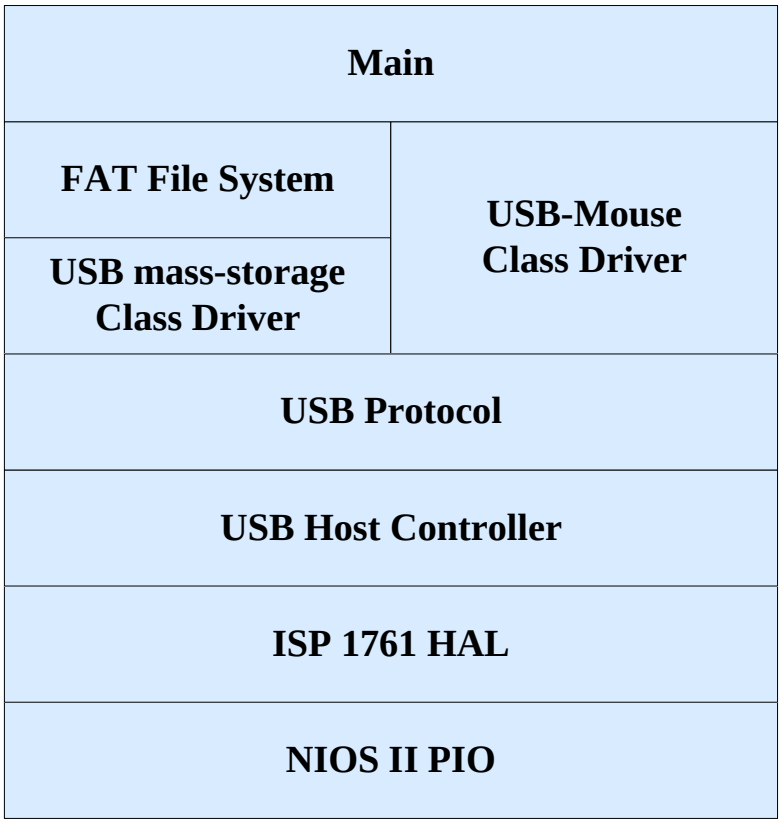


Figure 5.2. Software Stack of the USB-Host Demonstration

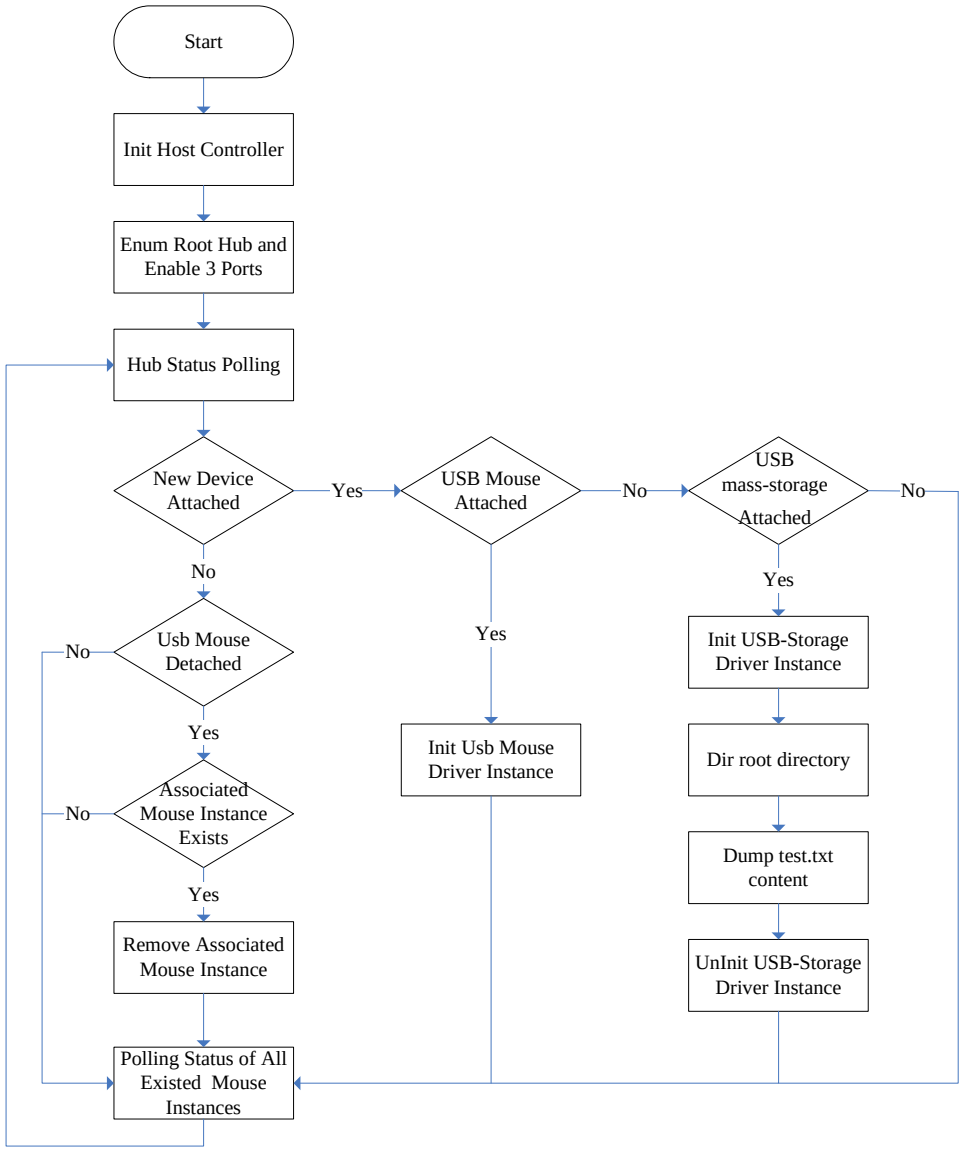


Figure 5.3. Software workflow of the USB-Host Demonstration

■ Demonstration Source Code

Quartus II Project directory: *DE3_USB*
FPGA Bit Stream: *DE3_USB.sof*
NIOS II Workspace: *DE3_USB\Software\Project_Usb_Host*

The NIOS II source code list is shown in Figure 5.4. Users can modify *terasic_debug.h* to configure the debug message. Note, debug message may effects the USB performance, and possibly causes malfunction in this demonstration.

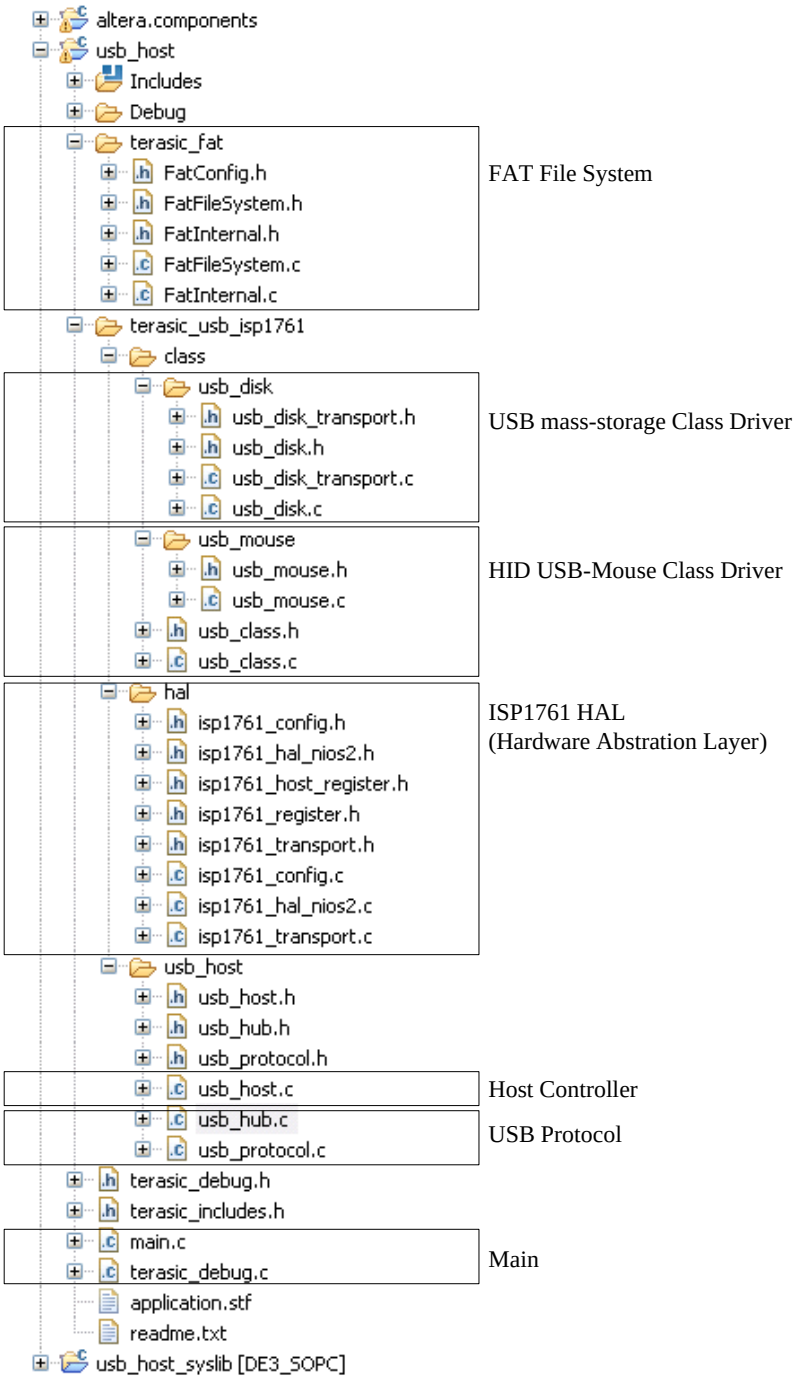


Figure 5.4. Source Code List of the USB-Host Demonstration

■ Demonstration Batch File

Demo Batch File Folder: *DE3_USB \Demo_Batch\usb_host*

The demo batch file folders include the following files:

- Batch File: *de3_usb_host.bat*, *de3_usb_host_bashrc*
- FPAG Configuration File: *DE3_USB.sof*
- NIOS II Program: *usb_host.elf*

Demonstration Setup

- Make sure Quartus II and NIOS II are installed.
- Power on DE3.
- Connect USB cable to DE3. The PC will need to install the USB Blaster driver for the first time use.
- Execute the demo batch file "*de3_usb_host.bat*" under the batch file folder, DE3_USB\demo_batch\usb_host.
- The LED of the three USB ports will be light after USB ports are configured completed.
- For USB mass-storage demonstration, copy test files to the root directory of USB-Disk.
- Plug USB mass-storage device or HID USB-Mouse into the USB ports in DE3, as shown in Figure 5.5.
- The device information will be displayed in nios2-terminal, as shown in Figure 5.6.

Reference

- ISP1761 Hi-Speed Universal Bus On-The-Go controller, Rev. 04 – 5 March 2007.
- Universal Serial Bus Specification, Revision 2.0, April 27, 2000.
- Enhanced Host Controller Interface Specification for Universal Serial Bus, Revision 1.0, March 12, 2002.
- Universal Serial Bus Mass Storage Class, Bulk-Only Transport, Revision 1.0, September 31, 1999.
- Universal Serial Bus Mass Storage Class, UFI Command Specification, Revision 1.0, December 14, 1998.
- Universal Serial Bus, Device Class Definition for Human Interface Devices (HID), Version 1.11, June 27, 2001.

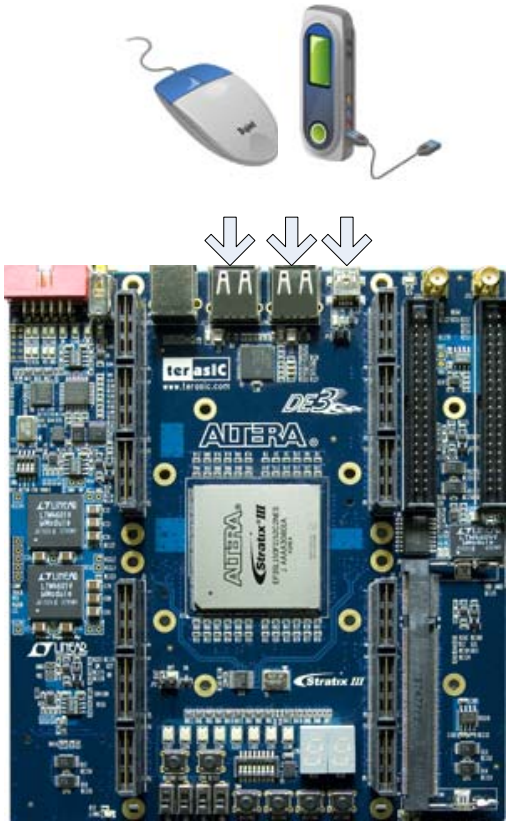


Figure 5.5. Plug USB-Devices into DE3

Figure 5.6. Display Device Information

5.2 USB Device

Most USB applications and products operate as USB devices, rather than USB hosts. This demonstration will show how the DE3 board can operate as a USB device, and be connected to a host computer. In this demonstration, the USB port 1 (mini-AB port) on DE3 is configured as a device port to connect with a host computer. The NIOS II processor communicates with host computer through USB Bulk Transfer with user-defined command sets. The USB device driver is implemented in NIOS C code. From the host computer side, a test program is used to communicate with DE3. The test program can configure LED status and poll button status through the USB connection.

The hardware system block diagram of this demonstration is the same as the USB Host. Figure 5.7 shows the NIOS II software stack of this demonstration. NIOS PIO block is provided from NIOS II System. The block provides basic I/O functions IORD and IOWR to access hardware directly. The function prototypes are defined in the header file <io.h>. The ISP 1761 HAL block implements functions to access internal control/data registers of the USB chip ISP 1761. USB Peripheral controller block implements control functions for ISP1761 Peripheral Controller. USB protocol block implements USB protocol. USB Bulk Driver implements a device driver to provide two bulk end-points, namely Bulk-In and Bulk-Out. Main program is implemented to communicate with a host computer. It calls bulk-read function to receive commands from the host computer, and calls bulk-write function to return data to the host computer.

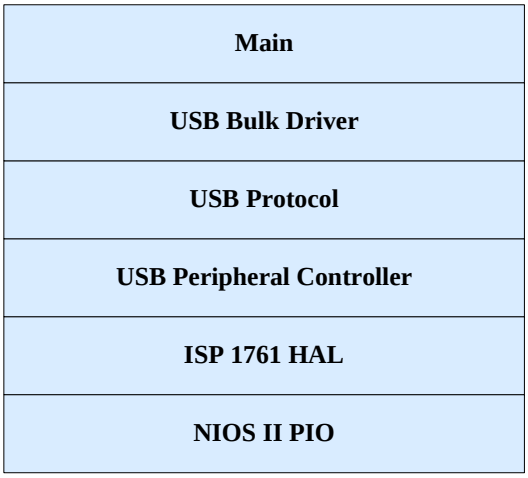


Figure 5.7. Software Stack of the USB-Device Demonstration

In the host computer, a test program named DE3_UsbControl.exe is used to communicate with DE3, as shown in Figure 5.8. At the first time when the host when computer connected to DE3 USB device port, a dialog will pop up to request a USB driver to be installed. The driver is available in the current demo folder, named *terasic_usb.sys* and *terasic_usb.inf*. After the driver is installed, users can launch the test program to communicate with the DE3.

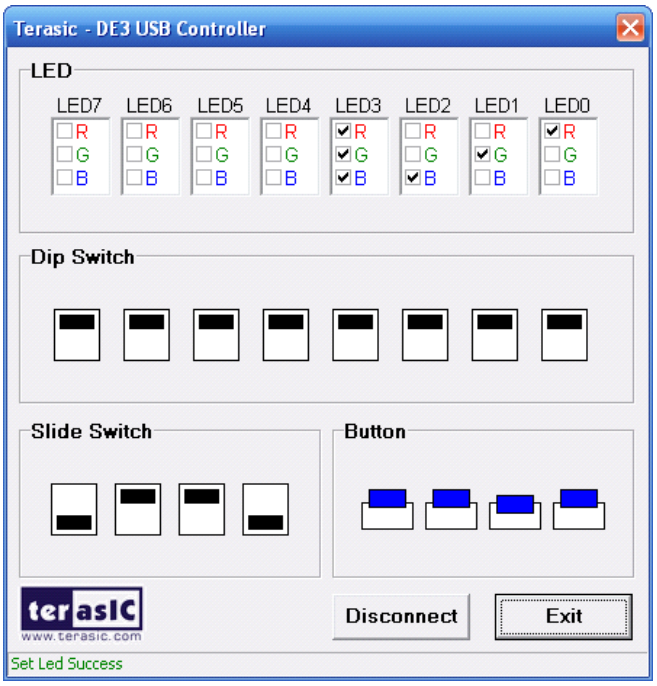


Figure 5.8. User Interface of the DE3_UsbControl.exe

■ Demonstration Source Code

Quartus Project directory: *DE3_USB*
FPGA Bit Stream: *DE3_USB.sof*
NIOS II Workspace: *DE3_USB\Software\Project_Usb_Device*

The NIOS II source code list is shown in Figure 5.9. Users can modify terasic_debug.h to configure the debug message. Note that any debug message may affect the USB performance, or even cause malfunction in this demonstration.

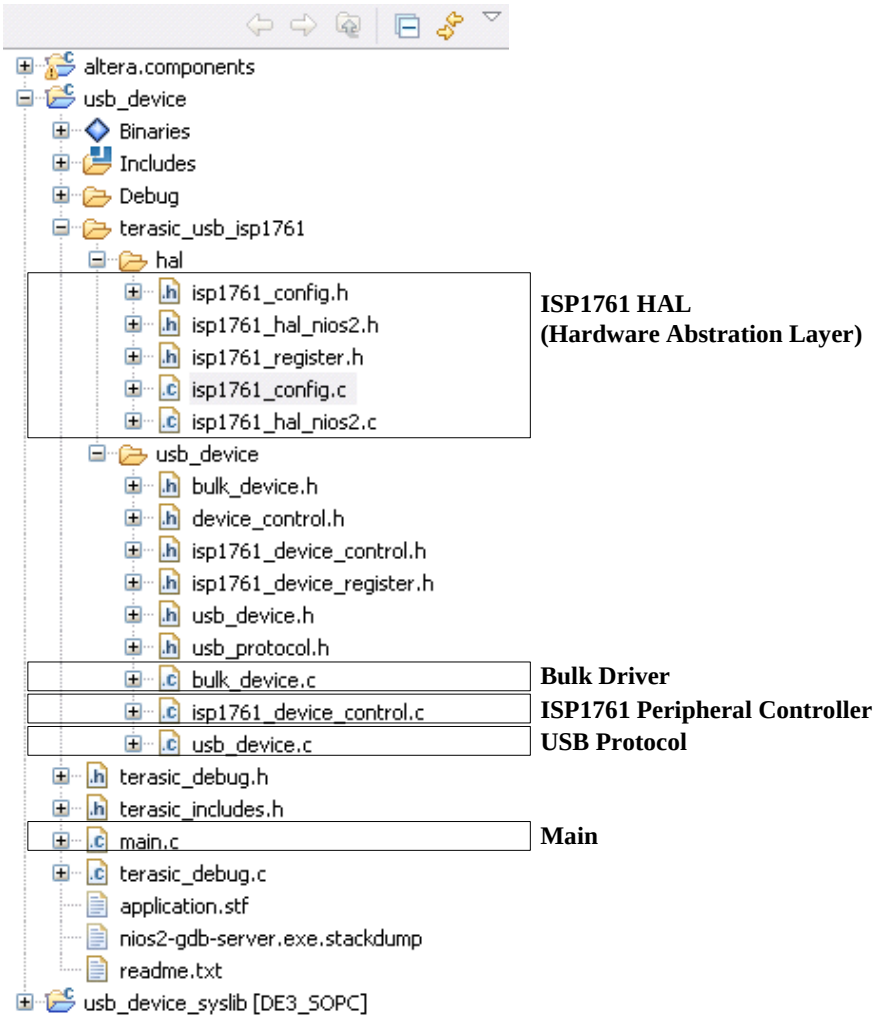


Figure 5.9. Source Code List of the USB-Device Demonstration

■ Demonstration Batch File

Demo Batch File Folder: *DE3_USB \demo_batch\usb_device*

The demo batch file includes the following files:

- Batch File: *de3_usb_device.bat, de3_usb_device_bashrc*
- FPAG Configure File: *DE3_USB.sof*
- NIOS II Program: *usb_device.elf*
- USB Driver for Windows XP: *terasic_usb.sys and terasic_usb.inf*
- USB Test Program for Windows XP: *DE3_UsbControl.exe*

■ Demonstration Setup

- It is suggested to run this demonstration under Windows XP.

- Make sure Quartus II and NIOS II are installed.
- Power on the DE3 board.
- Connect USB Blaster to DE3 board and install driver for USB Blaster if necessary.
- Execute the demo batch file "*de3_usb_device.bat*" under the batch file folder, *DE3_USB\demo_batch\usb_device*.
- Users may remove the USB Blaster once the FPAG configuration is completed.
- Connect USB cable from a host computer to the mini-AB port in DE3, as shown in Figure 5.10.
- For the first time the USB port of the host computer is connected to the min-AB port of the DE3 board, a dialog will pop up to request a USB driver to be installed. The required driver is available in the demo batch folder, *DE3_USB\demo_batch\usb_device*.
- Launch *DE3_UsbControl.exe* under the batch file folder, *DE3_USB\demo_batch\usb_device*.
- Click "**Connect**" in DE3_UsbControl window.
- After connection established, the button status in DE3 will be updated to the program interface, and users can start to configure the LED status now.

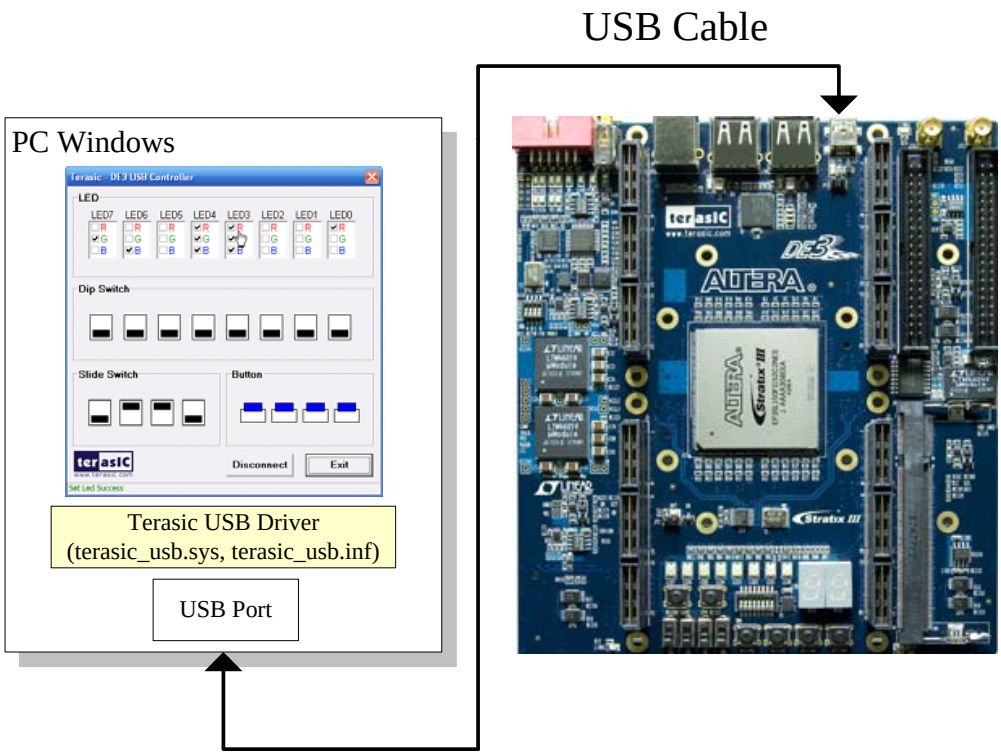


Figure 5.10. Connect USB ports for the USB-Device Demonstration.

5.3 SD Card

Many applications use a large external storage device, such as a SD card or CF card, to store data. The DE3 board provides the hardware and software needed for SD card access. In this

demonstration we will show how to browse files stored in the root directory of a SD card and how to read the file contents of a specific file. The SD card is required to be formatted as FAT File System in advance. Long file name is supported in this demonstration.

Figure 5.11 shows the hardware system block diagram of this demonstration. The system requires a 50 MHz clock provided from the board. The PLL generates a 100 MHz clock for the NIOS II processor and other controllers. Four PIO pins are connected to the SD card socket. SD 1-bit Mode is used to access the SD card hardware. The SD 1-bit protocol and FAT File System function are all implemented by NIOS II software. The software is stored in the on-chip memory.

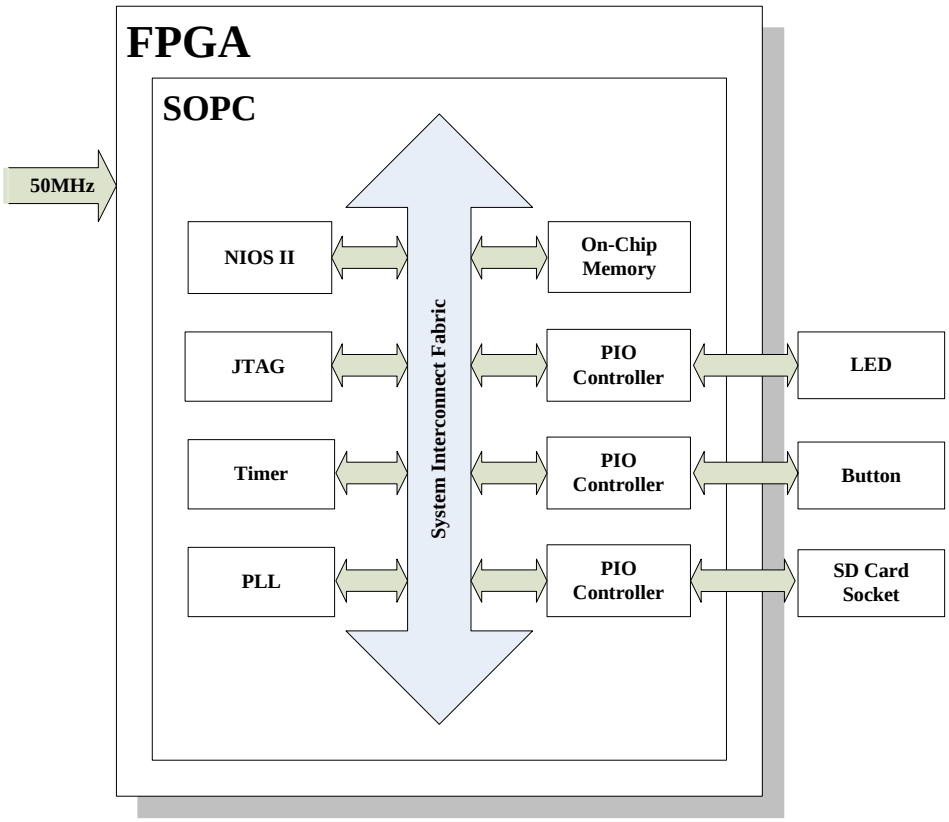


Figure 5.11. Block Diagram of the SD Card Demonstration

Figure 5.12 shows the software stack of this demonstration. The NIOS PIO block provides basic IO functions to access hardware directly. The functions are provided from NIOS II system and the function prototype is defined in the header file <io.h>. The SD-CARD block implements SD 1-bit mode protocol for communication with SD cards. The FAT File System block implements reading function for FAT16 and FAT 32 file system. Long filename is supported. By calling the exported FAT functions, users can browse files under the root directory of the SD card. Furthermore, users

can open a specified file and read the contents of the file.

The main block implements main control of this demonstration. When the program is executed, it detects whether a SD card is inserted. If a SD card is found, it will check whether the SD card is formatted as FAT file system. If a FAT file system is found, it searches all files in the root directory of the FAT file system and displays their names in the nios2-terminal. If a text file named “test.txt” is found, it will dump the file contents. If it successfully recognizes the FAT file system, it will turn on the green LED. On the other hand, it will turn on the red LED if it fails to parse the FAT file system or if there is no SD card found in the SD Card socket of the DE3 board. If users press BUTTON3 of the DE3 board, the program will perform above process again.

Figure 5.12. Software Stack of the SD Card Demonstration

■ Demonstration Source Code

- Project directory: *DE3_SDCARD*
- Bit stream used: *DE3_SDCARD.sof*
- NIOS II Workspace: *DE3_SDCARD\Software*

■ Demonstration Batch File

Demo Batch File Folder: *DE3_SDCARD \Demo_Batch*
The demo batch file includes following files:

- Batch File: de3_sdcard.bat, de3_sdcard_bashrc
- FPAG Configure File: DE3_SDCARD.sof
- NIOS II Program: DEMO_SDCARD.elf

■ Demonstration Setup

- Make sure Quartus II and NIOS II are installed on your PC.
- Power on the DE3 board.
- Connect USB Blaster to the DE3 board and install USB Blaster driver if necessary.
- Execute the demo batch file "*de3_sdcard.bat*" under the batch file folder, *DE3_SDCARD\demo_batch*.
- After NIOS II program is downloaded and executed successfully, a prompt message will be displayed in nios2-terminal
- Copy test files to the root directory of the SD Card.
- Insert the SD card into the SD Card socket of DE3, as shown in Figure 5.13.
- Press **Button3** of the DE3 board to start reading SD Card.
- The program will display SD Card information, as shown in Figure 5.14.

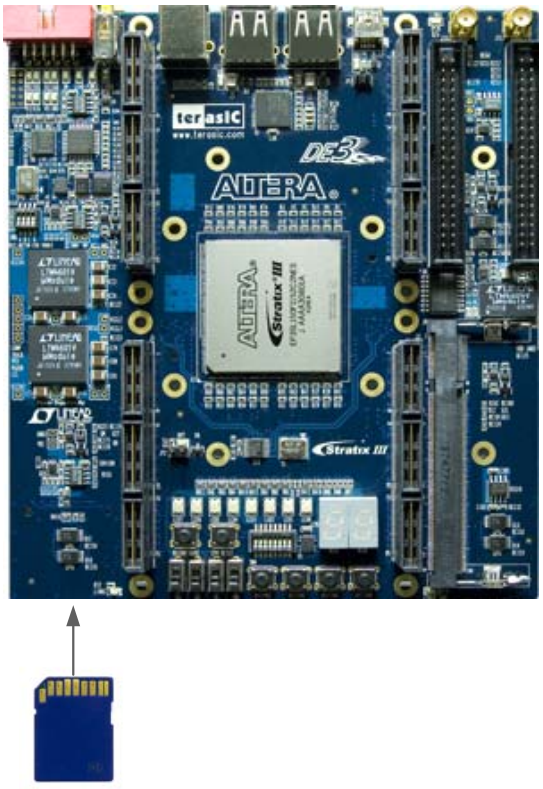


Figure 5.13. Insert SD Card for the SD-Card Demonstration

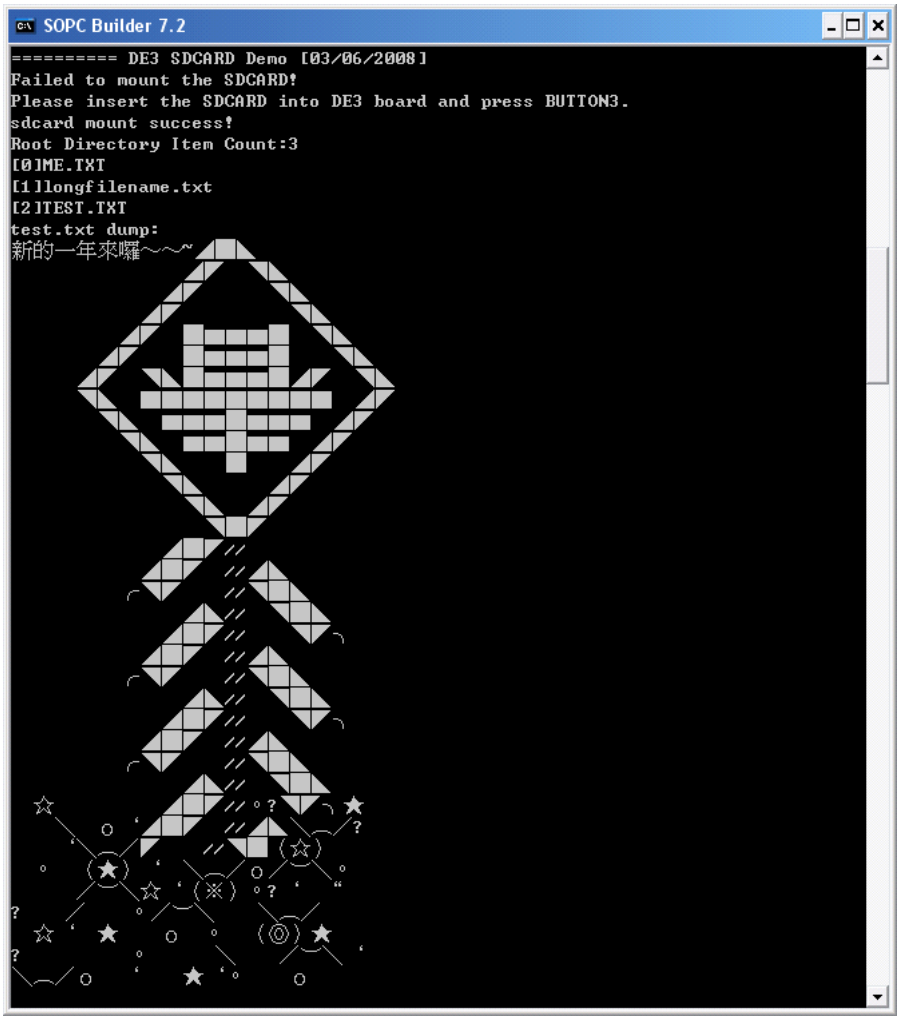


Figure 5.14. Display SD Card Information for the SD Card Demonstration

5.4 DDR2 SDRAM

Many applications use a high performance RAM, such as a DDR2 SDRAM, as temporary storage. The DE3 board provides the hardware and software designs for accessing DDR2 SDRAM SODIMM. In this demonstration, we show how to use Altera's "DDR2 SDRAM High Performance Controller" IP to build DDR2-SDRAM controller, and how to use NIOS processor to read and write the SDRAM for hardware verification. The required DDR2-SDRAM SODIMM module should be 256M-Bytes DDR2-533 at least. In the demonstration, we only provide 256M-Bytes accessing for SDRAM due to SOPC builder limitation. For none SOPC project, users can change the DDR2 IP setting to support higher capacity of SDRAM.

Figure 5.15 shows the system block diagram of this demonstration. The system requires a 50 MHz clock provided from the board. The DDR2 controller is configured as a 256M-Bytes DDR2-533 controller. The DDR2 IP generates one 266.667 MHZ clock as SDRAM's data clock and one half-rate system clock 133.333 MHZ for those controllers, e.g. NIOS processor, accessing the SDRAM. In the SOPC, NIOS and On-Chip Memory are designed running with the 133.333 MHZ clock, and the other controllers are designed running with 20 MHZ clock which is generated by the PLL. The NIOS program is running in the 128K-Bytes on-chip memory.

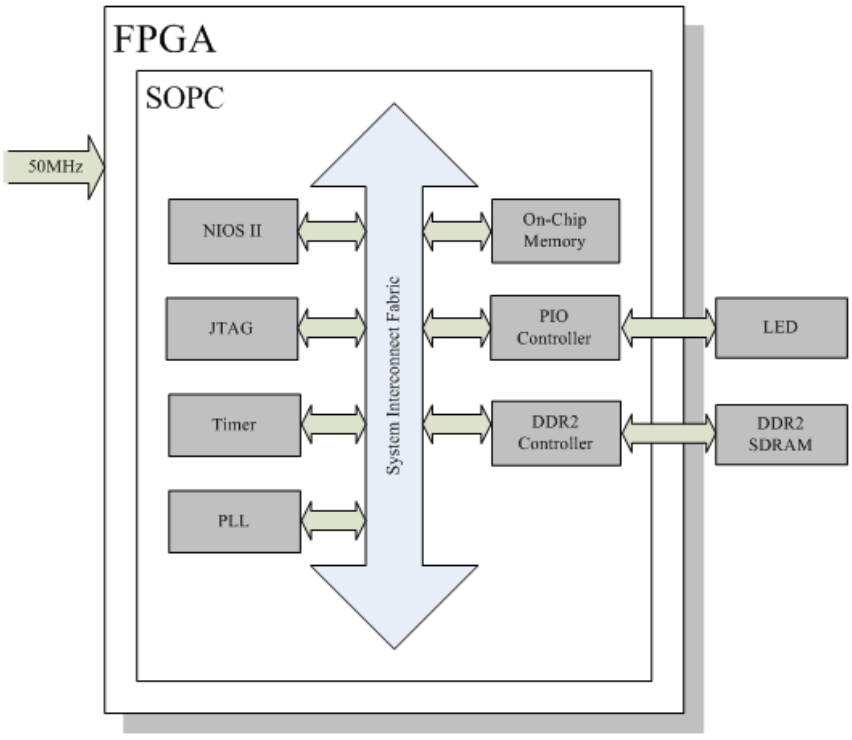


Figure 5.15. Block Diagram of the DDR2 Demonstration

The system flow is controlled by a NIOS program. First, the NIOS program writes test patterns into the whole 256M-Bytes SDRAM by calling standard library function – “memcpy”. Then, it calls NIOS system function, alt_dache_flush_all, to make sure all data has been written to SDRAM. Finally, it calls “memcpy” again to read data from SDRAM for data verification. The program will show progress in JTAG-Terminal when writing/reading data to/from the SDRAM. When verification process is completed, the result is displayed in the JTAG-Terminal.

■ Altera DDR2 SDRAM High Performance Controller

To use Altera DDR2 contrroler, users need to perform three major steps: 1). Create correct pin assignment for DDR2. 2). Setup correct parameters in DDR2 controller dialog. 3). Execute TCL files, generated by DDR2 IP, under your quartus project.

1. Pin Assignments

DE3_System builder can help users quickly generate accuracy pin assignments for DDR2. For DE3 configuration, select “DDR2-SO-DIMM” type, as shown Figure 5.16. For DDR2 configuration, select “Altera DDR2 IP” Pin Name, as shown Figure 5.17. Then,

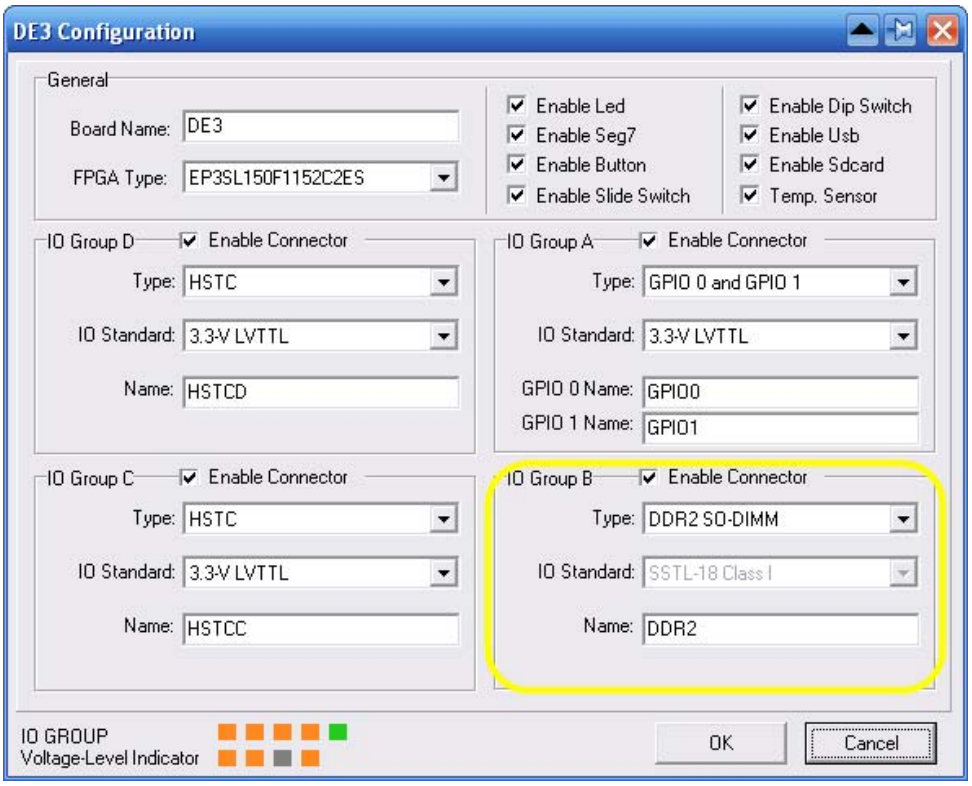


Figure 5.16. Select DDR2 SO-DIMM Type in DE3 Configuration

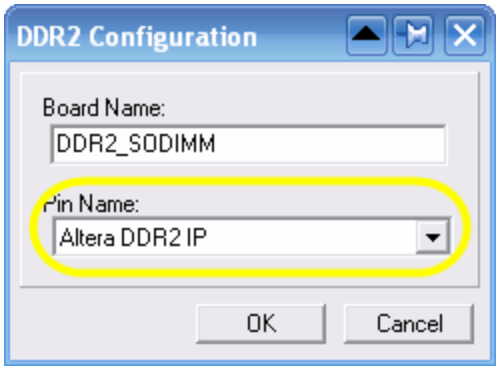


Figure 5.17. Select Altera DDR2 IP in DDR2 Configuration

2. DDR2 Parameter Settings

Figure 5.18 shows Memory Settings for DDR2 controller. The controller is configured as DDR2-SDRAM, 266.667 MHZ, 64-bits width, Un-buffered DIMM, CAS 5.0, 1 DIMM. To see the detail parameter information, as showing in Figure 5.19, users can click "modify parameters…" button. User can change the SDRAM capacity in this setting dialog.

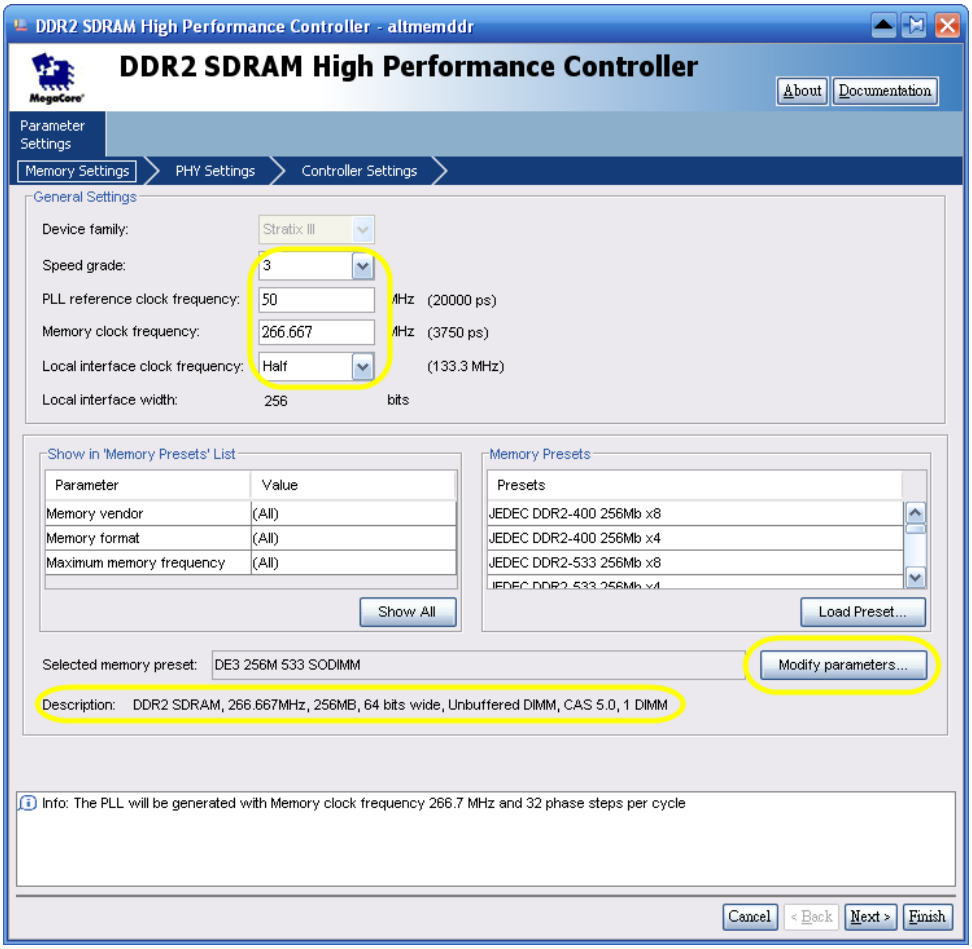


Figure 5.18. Memory Settings in DDR2 Controller

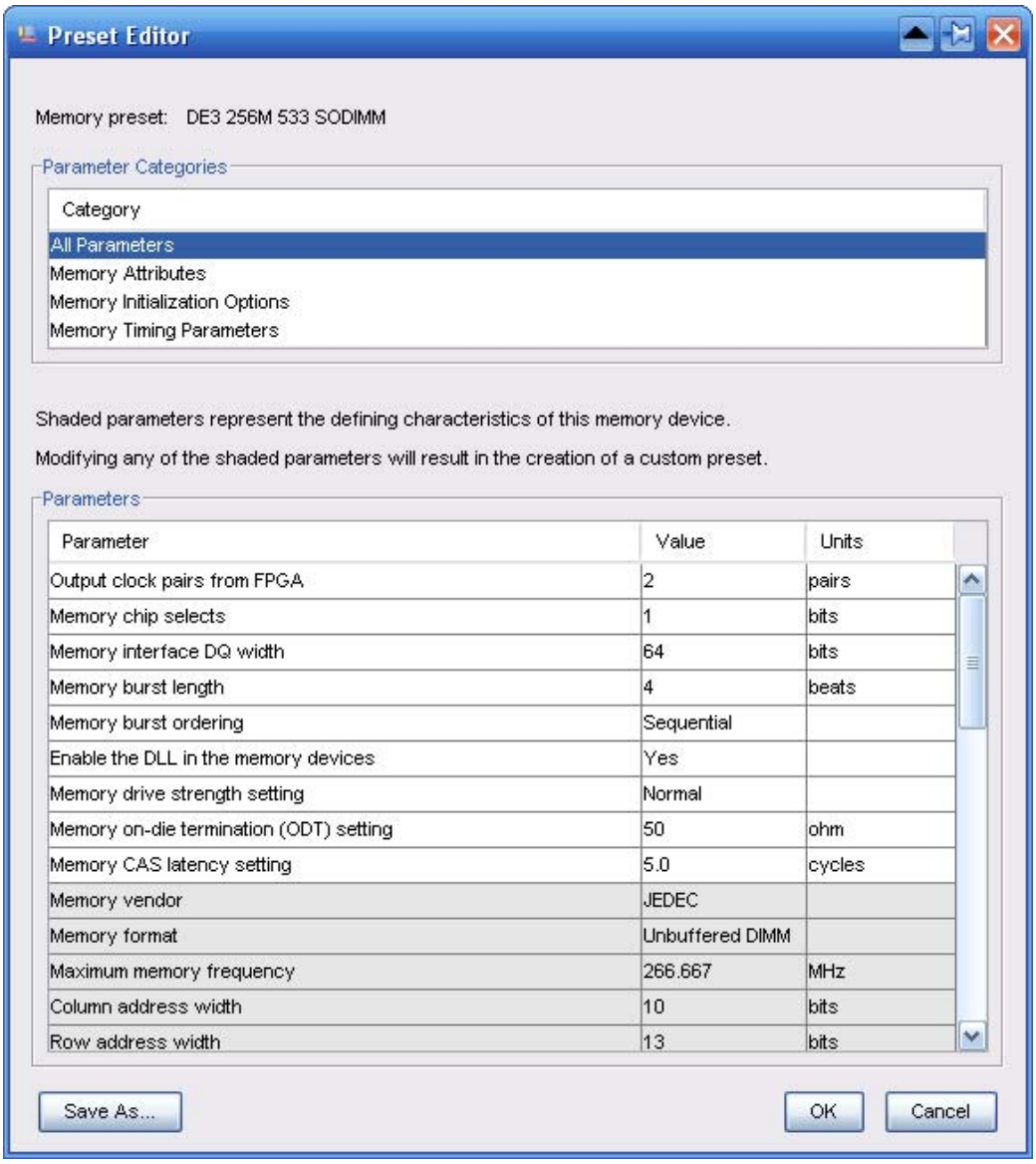


Figure 5.19. Parameter Settings in DDR2 Controller

Figure 5.20 shows PHY Settings for DDR2 controller. OCT and Differential DQS is enabled and Board skew set as 50 ps.

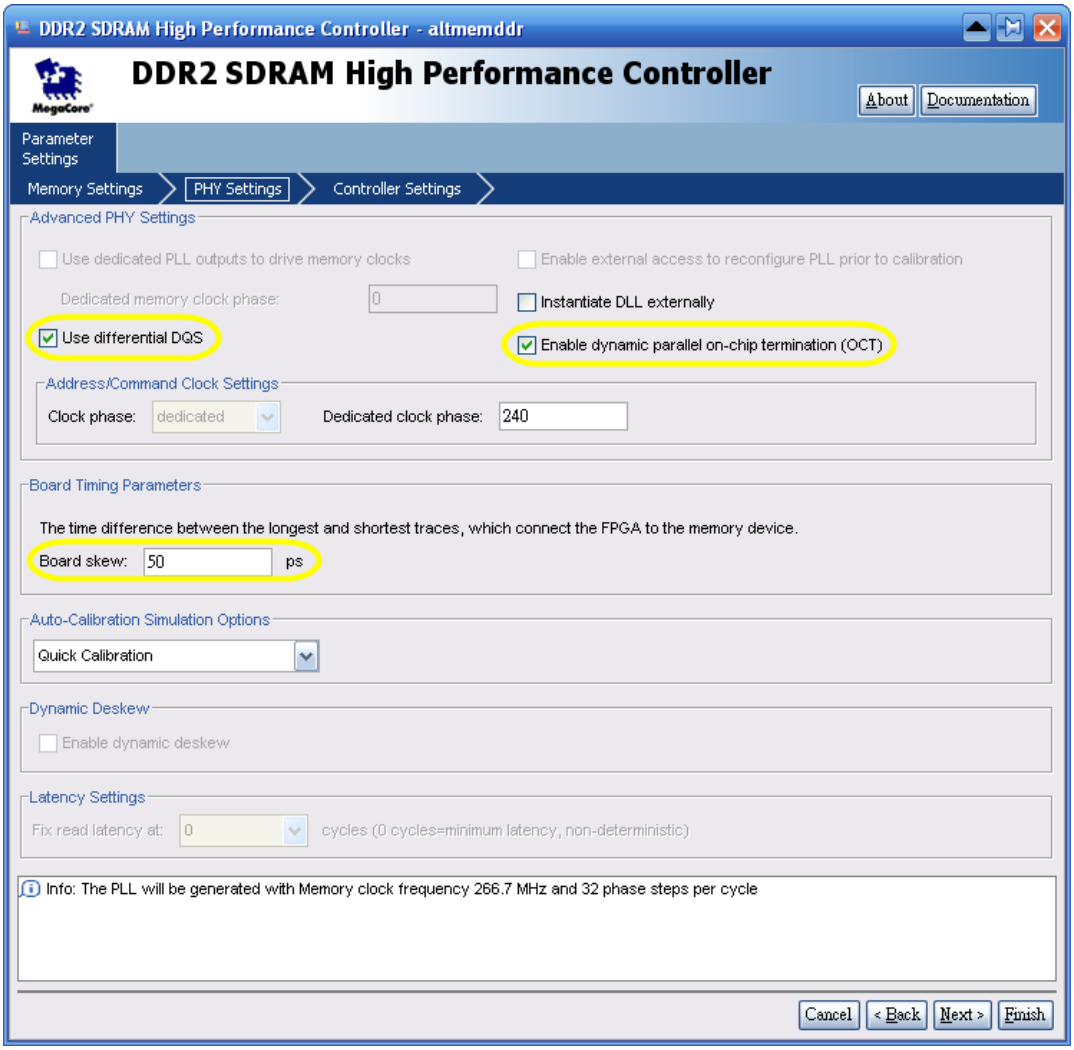


Figure 5.20. PHY Settings in DDR2 Controller

3. Execute DDR2 TCL Files

When DDR2 controller is created, the IP will generate some TLC files. Users must execute these TCL file first before start compiling, otherwise, Quartus will report error while compile. To execute DDR2 TCL file, click "Tools→ Tcl Script…" to popup TCL scripts dialog, as shown in Figure 5.21 . Then, execute the three marked TCl files individually.

Figure 5.21. Execute TCL under Quartus

■ Demonstration Source Code

- Project directory: *DE3_DDR2*
- Bit stream used: *DE3_DDR2.sof*
- NIOS II Workspace: *DE3_DDR2\Software*

■ Demonstration Batch File

Demo Batch File Folder: *DE3_DDR2 \Demo_Batch*
The demo batch file includes following files:

- Batch File: de3_ddr2.bat, de3_ddr2_bashrc
- FPAG Configure File: DE3_DDR2_Q8.sof
- NIOS II Program: DDR2_TEST.elf

■ Demonstration Setup

- Make sure Quartus II and NIOS II are installed on your PC.
- Make sure DDR2-SDRAM SODIMM is installed on your DE3 board, as shown in Figure 5.13.
- Power on the DE3 board.
- Connect USB Blaster to the DE3 board and install USB Blaster driver if necessary.
- Execute the demo batch file "*de3_ddr2.bat*" under the batch file folder, *DE3_DDR2\demo_batch*.
- After NIOS II program is downloaded and executed successfully, a prompt message will be displayed in nios2-terminal
- Press **Button1** or **Button0** of the DE3 board to start SDRAM verify process.
- The program will display progressing and result information, as shown in Figure 5.14.

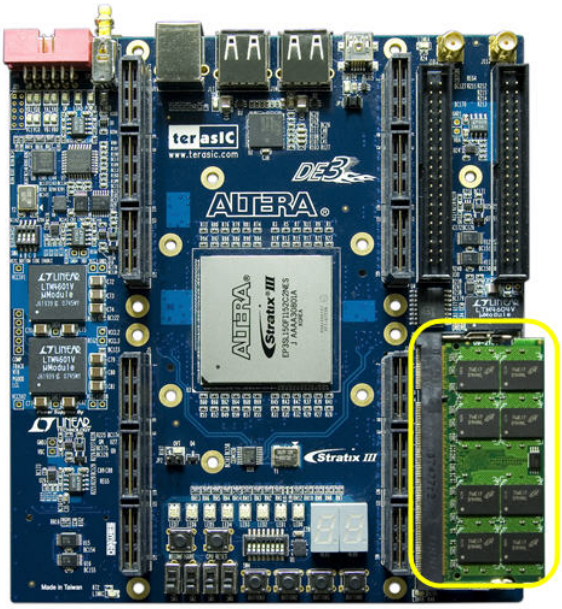


Figure 5.22. Insert DDR2-SDRAM SODIMM for the DDR2 Demonstration

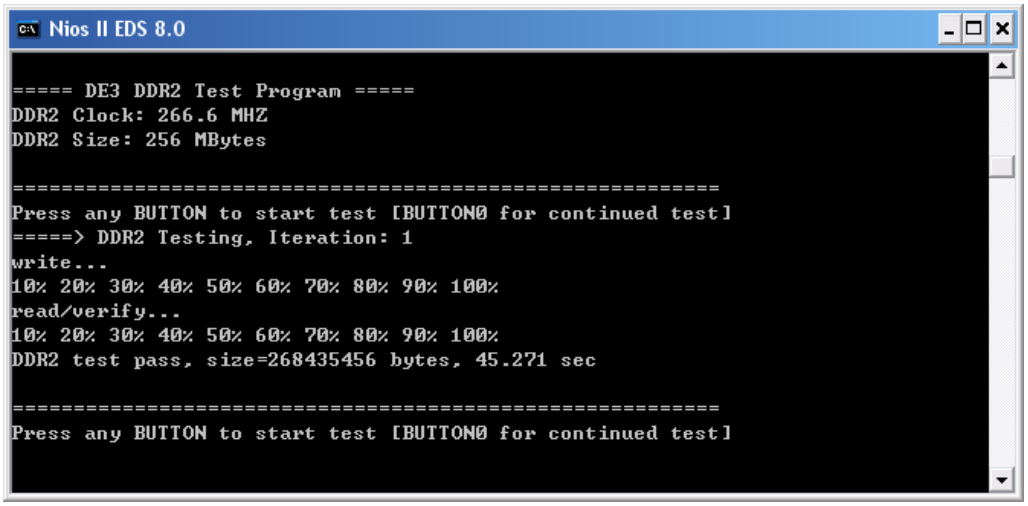


Figure 5.23. Display Progress and Result Information for the DDR2 Demonstration

Appendix A

Pin connections between components and FPGA on the DE3 board

This appendix lists the connections between components and Stratix III FPGA on the DE3 board.

■ Push-Button Switches

Table A-1. Push-button switches pinout with FPGA

Board Reference	Signal Name	FPGA Pin No.	I/O Standard	Description
BUTTON0	BUTTON[0]	K1	3.3V	High Logic Level when it is not pressed
BUTTON1	BUTTON[1]	K2	3.3V	High Logic Level when it is not pressed
BUTTON2	BUTTON[2]	M4	3.3V	High Logic Level when it is not pressed
BUTTON3	BUTTON[3]	M3	3.3V	High Logic Level when it is not pressed
CPU RESET	CPU_RST_N	U31	3.3V	User reset push-button
RECONFIGURE	nCONFIG	AE25	3.3V	System re-configuration push-button

■ Slide Switches

Table A-2 Slide Switches pinout with FPGA

Board Reference	Signal Name	FPGA Pin No.	I/O Standard	Description
SW0	SW0	W5	3.3V	High Logic Level when SW is in upper position
SW1	SW1	W6	3.3V	High Logic Level when SW is in upper position
SW2	SW2	W9	3.3V	High Logic Level when SW is in upper position
SW3	SW3	W11	3.3V	High Logic Level when SW is in upper position

8-Position Dip Switch

Table A-3 8-Position DIP switch pinout with FPGA

Board Reference	Signal Name	FPGA Pin No.	I/O Standard	Description
SW4	DIP_SW0	R12	3.3V	High Logic Level when SW is in down position
SW4	DIP_SW1	P5	3.3V	High Logic Level when SW is in down position
SW4	DIP_SW2	R4	3.3V	High Logic Level when SW is in down position
SW4	DIP_SW3	R3	3.3V	High Logic Level when SW is in down position
SW4	DIP_SW4	P2	3.3V	High Logic Level when SW is in down position
SW4	DIP_SW5	R1	3.3V	High Logic Level when SW is in down position
SW4	DIP_SW6	T2	3.3V	High Logic Level when SW is in down position
SW4	DIP_SW7	T1	3.3V	High Logic Level when SW is in down position

RGB LEDs

Table A-4 RGB LEDs pinout with FPGA

Board Reference	Signal Name	FPGA Pin No.	I/O Standard	Description
LED0	LEDR[0]	AD1	3.3V	Red color of LED0
LED1	LEDR[1]	AC1	3.3V	Red color of LED1
LED2	LEDR[2]	AC2	3.3V	Red color of LED2
LED3	LEDR[3]	AB2	3.3V	Red color of LED3
LED4	LEDR[4]	AC4	3.3V	Red color of LED4
LED5	LEDR[5]	AB4	3.3V	Red color of LED5
LED6	LEDR[6]	AA3	3.3V	Red color of LED6
LED7	LEDR[7]	AB3	3.3V	Red color of LED7
LED0	LEDG[0]	AB1	3.3V	Green color of LED0
LED1	LEDG[1]	AA1	3.3V	Green color of LED1
LED2	LEDG[2]	Y1	3.3V	Green color of LED2
LED3	LEDG[3]	Y2	3.3V	Green color of LED3
LED4	LEDG[4]	Y3	3.3V	Green color of LED4
LED5	LEDG[5]	W3	3.3V	Green color of LED5
LED6	LEDG[6]	AA4	3.3V	Green color of LED6
LED7	LEDG[7]	Y4	3.3V	Green color of LED7
LED0	LEDB[0]	AB5	3.3V	Blue color of LED0

LED1	LEDB[1]	AB6	3.3V	Blue color of LED1
LED2	LEDB[2]	AA6	3.3V	Blue color of LED2
LED3	LEDB[3]	AA7	3.3V	Blue color of LED3
LED4	LEDB[4]	Y7	3.3V	Blue color of LED4
LED5	LEDB[5]	Y8	3.3V	Blue color of LED5
LED6	LEDB[6]	Y9	3.3V	Blue color of LED6
LED7	LEDB[7]	Y10	3.3V	Blue color of LED7

■ 7-Segment Display

Table A-5 7-Segment Display pinout with FPGA

Board Reference	Signal Name	FPGA Pin No.	I/O Standard	Description
HEX0	HEX0_DP	V3	3.3V	Seven Segment Decimal Point 0
HEX0	HEX0_D0	W12	3.3V	Seven Segment Digit 0[0]
HEX0	HEX0_D1	Y11	3.3V	Seven Segment Digit 0[1]
HEX0	HEX0_D2	W10	3.3V	Seven Segment Digit 0[2]
HEX0	HEX0_D3	W8	3.3V	Seven Segment Digit 0[3]
HEX0	HEX0_D4	W7	3.3V	Seven Segment Digit 0[4]
HEX0	HEX0_D5	Y5	3.3V	Seven Segment Digit 0[5]
HEX0	HEX0_D6	Y6	3.3V	Seven Segment Digit 0[6]
HEX1	HEX1_DP	V4	3.3V	Seven Segment Decimal Point 1
HEX1	HEX1_D0	P3	3.3V	Seven Segment Digit 1[0]
HEX1	HEX1_D1	N4	3.3V	Seven Segment Digit 1[1]
HEX1	HEX1_D2	N3	3.3V	Seven Segment Digit 1[2]
HEX1	HEX1_D3	N1	3.3V	Seven Segment Digit 1[3]
HEX1	HEX1_D4	M1	3.3V	Seven Segment Digit 1[4]
HEX1	HEX1_D5	L1	3.3V	Seven Segment Digit 1[5]
HEX1	HEX1_D6	L2	3.3V	Seven Segment Digit 1[6]

HSTC Connectors

Table A-6 The odd pins of bank1 on HSTC connectors pinout with FPGA							
Board Reference	Signal Name	FPGA Pin No.				I/O Standard	Description
		HSTC A(J1)	HSTC B(J3)	HSTC C(J5)	HSTC D(J7)		
3	CLKOUT_n0	AE19	AD16	L16	L20	Configurable	HSTC connector CLKOUT n0
5	CLKOUT_p0	AD19	AD15	K16	L19	Configurable	HSTC connector CLKOUT p0
9	TX_n0	AC26	AE7	L8	J30	Configurable	HSTC connector IO TX_n[0]
11	TX_p0	AC25	AE8	L9	J29	Configurable	HSTC connector IO TX_p[0]
15	TX_n1	AD27	AF5	M9	K28	Configurable	HSTC connector IO TX_n[1]
17	TX_p1	AD26	AF6	M10	K27	Configurable	HSTC connector IO TX_p[1]
21	TX_n2	AE28	AC8	K7	N25	Configurable	HSTC connector IO TX_n[2]
23	TX_p2	AE27	AC9	K8	M24	Configurable	HSTC connector IO TX_p[2]
27	TX_n3	AF29	AE5	J6	M27	Configurable	HSTC connector IO TX_n[3]
29	TX_p3	AF28	AE6	J7	M26	Configurable	HSTC connector IO TX_p[3]
33	TX_n4	AD29	AB10	N10	K30	Configurable	HSTC connector IO TX_n[4]
35	TX_p4	AD28	AC11	N11	K29	Configurable	HSTC connector IO TX_p[4]
39	TX_n5	AE30	AD6	K5	L29	Configurable	HSTC connector IO TX_n[5]
41	TX_p5	AE29	AD7	K6	L28	Configurable	HSTC connector IO TX_p[5]
45	TX_n6	AB27	AC7	N8	M28	Configurable	HSTC connector IO TX_n[6]
47	TX_p6	AB26	AB8	N9	N27	Configurable	HSTC connector IO TX_p[6]
51	TX_n7	AB25	AB9	L6	N26	Configurable	HSTC connector IO TX_n[7]
53	TX_p7	AB24	AA10	L7	P25	Configurable	HSTC connector IO TX_p[7]
57	TX_n8	AD31	AC5	L4	L32	Configurable	HSTC connector IO TX_n[8]
59	TX_p8	AD30	AC6	L5	L31	Configurable	HSTC connector IO TX_p[8]

Table A-7 The even pins of bank1 on HSTC connectors pinout with FPGA							
Board Reference	Signal Name	FPGA Pin No.				I/O Standard	Description
		HSTC A	HSTC B	HSTC C	HSTC D		
2	PSNT_n						HSTC connector present
4	CLKIN_n0	AE32	AE3	K3	J34	Configurable	HSTC connector CLKIN n0
6	CLKIN_p0	AE31	AE4	K4	J33	Configurable	HSTC connector CLKIN p0
10	RX_n0	AL33	AM1	D2	F32	Configurable	HSTC connector IO RX_n[0]
12	RX_p0	AL32	AM2	D3	F31	Configurable	HSTC connector IO RX_p[0]

16	RX_n1	AH31	AJ3	D1	C34	Configurable	HSTC connector IO RX_n[1]
18	RX_p1	AH30	AJ4	C1	C33	Configurable	HSTC connector IO RX_p[1]
22	RX_n2	AL34	AL1	G4	H32	Configurable	HSTC connector IO RX_n[2]
24	RX_p2	AM34	AL2	G5	H31	Configurable	HSTC connector IO RX_p[2]
28	RX_n3	AJ32	AG3	F3	D34	Configurable	HSTC connector IO RX_n[3]
30	RX_p3	AJ31	AG4	F4	D33	Configurable	HSTC connector IO RX_p[3]
34	RX_n4	AK34	AK1	E1	J32	Configurable	HSTC connector IO RX_n[4]
36	RX_p4	AK33	AJ2	E2	J31	Configurable	HSTC connector IO RX_p[4]
40	RX_n5	AG32	AJ1	H3	E34	Configurable	HSTC connector IO RX_n[5]
42	RX_p5	AG31	AH2	H4	F33	Configurable	HSTC connector IO RX_p[5]
46	RX_n6	AH34	AF3	G1	F34	Configurable	HSTC connector IO RX_n[6]
48	RX_p6	AJ34	AF4	F1	G33	Configurable	HSTC connector IO RX_p[6]
52	RX_n7	AF32	AH1	J3	K32	Configurable	HSTC connector IO RX_n[7]
54	RX_p7	AF31	AG1	J4	K31	Configurable	HSTC connector IO RX_p[7]
58	RX_n8	AG34	AF1	H1	G34	Configurable	HSTC connector IO RX_n[8]
60	RX_p8	AH33	AF2	G2	H34	Configurable	HSTC connector IO RX_p[8]

Table A-8 The odd pins of bank2 on HSTC connectors pinout with FPGA

Board Reference	Signal Name	FPGA Pin No.				I/O Standard	Description
		HSTC A	HSTC B	HSTC C	HSTC D		
63	CLKOUT_n1	AE18	AF16	K17	J19	Configurable	HSTC connector CLKOUT n1
65	CLKOUT_p1	AD18	AE16	L17	K19	Configurable	HSTC connector CLKOUT p1
69	TX_n9	AM21	AK15	A15	H20	Configurable	HSTC connector IO TX_n[9]
71	TX_p9	AP20	AG15	C14	E20	Configurable	HSTC connector IO TX_p[9]
75	TX_n10	AJ20	AN13	F15	A21	Configurable	HSTC connector IO TX_n[10]
77	TX_p10	AJ21	AP14	D15	A22	Configurable	HSTC connector IO TX_p[10]
81	TX_n11	AL22	AP13	D14	C23	Configurable	HSTC connector IO TX_n[11]
83	TX_p11	AM22	AM12	E13	B22	Configurable	HSTC connector IO TX_p[11]
87	TX_n12	AP26	AP11	A12	A26	Configurable	HSTC connector IO TX_n[12]
89	TX_p12	AP23	AP9	A9	A24	Configurable	HSTC connector IO TX_p[12]
93	TX_n13	AD21	AF15	K15	J20	Configurable	HSTC connector IO TX_n[13]
95	TX_p13	AE20	AE15	L14	K20	Configurable	HSTC connector IO TX_p[13]
99	TX_n14	AE22	AE14	K14	K22	Configurable	HSTC connector IO TX_n[14]
101	TX_p14	AE21	AE13	K13	K21	Configurable	HSTC connector IO TX_p[14]
105	TX_n15	AK24	AM11	D13	E25	Configurable	HSTC connector IO TX_n[15]
107	TX_p15	AL25	AK10	D10	C24	Configurable	HSTC connector IO TX_p[15]

111	TX_n16	AJ23	AP8	G13	C27	Configurable	HSTC connector IO TX_n[16]
113	TX_p16	AK22	AM8	E11	A27	Configurable	HSTC connector IO TX_p[16]
117	TX_n17	AH23	AM7	G12	A29	Configurable	HSTC connector IO TX_n[17]
119	TX_p17	AJ24	AP6	F11	C28	Configurable	HSTC connector IO TX_p[17]

Table A-9 The even pins of bank2 on HSTC connectors pinout with FPGA

Board Reference	Signal Name	FPGA Pin No.				I/O Standard	Description
		HSTC A	HSTC B	HSTC C	HSTC D		
64	CLKIN_n1	AP19	AP15	A16	A20	Configurable	HSTC connector CLKIN n1
66	CLKIN_p1	AN19	AN15	B16	B20	Configurable	HSTC connector CLKIN p1
70	RX_n9	AP21	AJ15	A14	F20	Configurable	HSTC connector IO RX_n[9]
72	RX_p9	AN21	AH15	B14	G20	Configurable	HSTC connector IO RX_p[9]
76	RX_n10	AP22	AJ14	A13	F21	Configurable	HSTC connector IO RX_n[10]
78	RX_p10	AN22	AH14	B13	G21	Configurable	HSTC connector IO RX_p[10]
82	RX_n11	AL21	AP12	E14	A23	Configurable	HSTC connector IO RX_n[11]
84	RX_p11	AK21	AN12	F14	B23	Configurable	HSTC connector IO RX_p[11]
88	RX_n12	AP24	AP10	A11	A25	Configurable	HSTC connector IO RX_n[12]
90	RX_p12	AN24	AN10	B11	B25	Configurable	HSTC connector IO RX_p[12]
94	RX_n13	AP25	AN9	A10	B26	Configurable	HSTC connector IO RX_n[13]
96	RX_p13	AN25	AM9	B10	C26	Configurable	HSTC connector IO RX_p[13]
100	RX_n14	AG21	AF14	H14	J21	Configurable	HSTC connector IO RX_n[14]
102	RX_p14	AF21	AF13	J14	J22	Configurable	HSTC connector IO RX_p[14]
106	RX_n15	AM23	AL12	C12	D24	Configurable	HSTC connector IO RX_n[15]
108	RX_p15	AL23	AK12	D12	D25	Configurable	HSTC connector IO RX_p[15]
112	RX_n16	AM24	AL11	C11	D23	Configurable	HSTC connector IO RX_n[16]
114	RX_p16	AL24	AL10	D11	E23	Configurable	HSTC connector IO RX_p[16]
118	RX_n17	AJ22	AP7	F12	A28	Configurable	HSTC connector IO RX_n[17]
120	RX_p17	AH22	AN7	F13	B28	Configurable	HSTC connector IO RX_p[17]

Table A-10 The odd pins of bank3 on HSTC connectors pinout with FPGA							
Board Reference	Signal Name	FPGA Pin No.				I/O Standard	Description
		HSTC A	HSTC B	HSTC C	HSTC D		
121	POWER_ON						The POWER ON control signal is to enable/diable I/O power from DE3. It will be kept as logic high always, except when DE3 control panel sends power-off command. This control signal can be neglected when designing your daughter card, if such functionality is not required.
123	CLKOUT_2	AA24	AD4	P11	M29	Configurable	HSTC connector CLKOUT 2
125	TDO						JTAG Data Out
129	TCK						JTAG Clock
131	SDA	V29	T9	T5	R30	3.3V	I2C Data
133	TX_n18	AM28	AJ13	A6	H23	Configurable	HSTC connector IO TX_n[18]
135	TX_p18	AP29	AG12	C7	F22	Configurable	HSTC connector IO TX_p[18]
137	TX_n19	AK25	AL8	E10	D27	Configurable	HSTC connector IO TX_n[19]
139	TX_p19	AM26	AJ10	D8	F25	Configurable	HSTC connector IO TX_p[19]
141	TX_n20	AK27	AJ9	D7	D28	Configurable	HSTC connector IO TX_n[20]
143	TX_p20	AL28	AL7	E8	F26	Configurable	HSTC connector IO TX_p[20]
145	TX_n21	AP32	AP5	A5	A33	Configurable	HSTC connector IO TX_n[21]
147	TX_p21	AP30	AP2	A3	A30	Configurable	HSTC connector IO TX_p[21]
149	TX_n22	AH25	AN6	J12	B29	Configurable	HSTC connector IO TX_n[22]
151	TX_p22	AF23	AM6	G10	C29	Configurable	HSTC connector IO TX_p[22]
153	TX_n23	AH26	AM4	J11	D31	Configurable	HSTC connector IO TX_n[23]
155	TX_p23	AF24	AL4	G9	C31	Configurable	HSTC connector IO TX_p[23]
157	TX_n24	AH27	AK6	C6	G27	Configurable	HSTC connector IO TX_n[24]
159	TX_p24	AJ27	AJ6	D6	F27	Configurable	HSTC connector IO TX_p[24]
161	TX_n25	AJ29	AF11	F9	K24	Configurable	HSTC connector IO TX_n[25]
163	TX_p25	AJ26	AE11	G8	J24	Configurable	HSTC connector IO TX_p[25]
165	TX_n26	AL29	AF10	F8	K25	Configurable	HSTC connector IO TX_n[26]
167	TX_p26	AM29	AE10	F6	J25	Configurable	HSTC connector IO TX_p[26]
169	TX_n27	AE24	AD13	M13	K23	Configurable	HSTC connector IO TX_n[27]
171	TX_p27	AE23	AE12	L13	L22	Configurable	HSTC connector IO TX_p[27]
173	TX_n28	AL20	AL13	C17	E22	Configurable	HSTC connector IO TX_n[28]

175	TX_p28	AM18	AK13	C15	D22	Configurable	HSTC connector IO TX_p[28]
177	TX_n29	AK18	AM15	D17	D20	Configurable	HSTC connector IO TX_n[29]
179	TX_p29	AL18	AL15	E17	C20	Configurable	HSTC connector IO TX_p[29]

Table A-11 The even pins of bank3 on HSTC connectors pinout with FPGA

Board Reference	Signal Name	FPGA Pin No.				I/O Standard	Description
		HSTC A	HSTC B	HSTC C	HSTC D		
124	CLKIN_2	AP18	AP16	A17	A19	Configurable	HSTC connector CLKIN 2
126	TDI						JTAG Data In
130	TMS						JTAG Mode Select
132	SCL	W28	T8	T4	R29	3.3V	I2C Clock
134	RX_n18	AP27	AJ12	A8	F23	Configurable	HSTC connector IO RX_n[18]
136	RX_p18	AN27	AH12	B8	G23	Configurable	HSTC connector IO RX_p[18]
138	RX_n19	AP28	AJ11	A7	F24	Configurable	HSTC connector IO RX_n[19]
140	RX_p19	AN28	AH11	B7	G24	Configurable	HSTC connector IO RX_p[19]
142	RX_n20	AL27	AL9	C9	D26	Configurable	HSTC connector IO RX_n[20]
144	RX_p20	AL26	AK9	D9	E26	Configurable	HSTC connector IO RX_p[20]
146	RX_n21	AP31	AP4	A4	A31	Configurable	HSTC connector IO RX_n[21]
148	RX_p21	AN31	AN4	B4	B31	Configurable	HSTC connector IO RX_p[21]
150	RX_n22	AP33	AP3	A2	A32	Configurable	HSTC connector IO RX_n[22]
152	RX_p22	AN33	AN3	B2	B32	Configurable	HSTC connector IO RX_p[22]
154	RX_n23	AH24	AM5	G11	C30	Configurable	HSTC connector IO RX_n[23]
156	RX_p23	AG24	AL5	H11	D30	Configurable	HSTC connector IO RX_p[23]
158	RX_n24	AN30	AK7	B5	E28	Configurable	HSTC connector IO RX_n[24]
160	RX_p24	AM30	AJ7	C5	F28	Configurable	HSTC connector IO RX_p[24]
162	RX_n25	AM32	AJ8	C3	E29	Configurable	HSTC connector IO RX_n[25]
164	RX_p25	AM31	AH8	C4	F29	Configurable	HSTC connector IO RX_p[25]
166	RX_n26	AM19	AM14	C16	C21	Configurable	HSTC connector IO RX_n[26]
168	RX_p26	AL19	AL14	D16	D21	Configurable	HSTC connector IO RX_p[26]
170	RX_n27	AD22	AD12	K11	L23	Configurable	HSTC connector IO RX_n[27]
172	RX_p27	AC22	AC12	K12	M23	Configurable	HSTC connector IO RX_p[27]
174	RX_n28	AK19	AM17	E16	C18	Configurable	HSTC connector IO RX_n[28]
176	RX_p28	AJ19	AL17	F16	D18	Configurable	HSTC connector IO RX_p[28]
178	RX_n29	AF20	AK16	J16	E19	Configurable	HSTC connector IO RX_n[29]
180	RX_p29	AF19	AJ16	J15	F19	Configurable	HSTC connector IO RX_p[29]

■ GPIO Expansion Header

Table A-12 GPIO Expansion Header 0 pinout with FPGA

Board Reference	Signal Name	FPGA Pin No.	I/O Standard	Description
J10-1	GPIO0_CLKINn0	AE32	Configurable	GPIO Expansion 0 Clock In
J10-3	GPIO0_CLKINp0	AE31	Configurable	GPIO Expansion 0 Clock In
J10-19	GPIO0_CLKOUTn0	AE19	Configurable	GPIO Expansion 0 PLL Out
J10-21	GPIO_CLKOUTp0	AD19	Configurable	GPIO Expansion 0 PLL Out
J10-2	GPIO0_D0	AL33	Configurable	GPIO Expansion 0 IO[0]
J10-4	GPIO0_D1	AL32	Configurable	GPIO Expansion 0 IO[1]
J10-5	GPIO0_D2	AL34	Configurable	GPIO Expansion 0 IO[2]
J10-6	GPIO0_D3	AH31	Configurable	GPIO Expansion 0 IO[3]
J10-7	GPIO0_D4	AM34	Configurable	GPIO Expansion 0 IO[4]
J10-8	GPIO0_D5	AH30	Configurable	GPIO Expansion 0 IO[5]
J10-9	GPIO0_D6	AK34	Configurable	GPIO Expansion 0 IO[6]
J10-10	GPIO0_D7	AJ32	Configurable	GPIO Expansion 0 IO[7]
J10-13	GPIO0_D8	AK33	Configurable	GPIO Expansion 0 IO[8]
J10-14	GPIO0_D9	AJ31	Configurable	GPIO Expansion 0 IO[9]
J10-15	GPIO0_D10	AH34	Configurable	GPIO Expansion 0 IO[10]
J10-16	GPIO0_D11	AG32	Configurable	GPIO Expansion 0 IO[11]
J10-17	GPIO0_D12	AJ34	Configurable	GPIO Expansion 0 IO[12]
J10-18	GPIO0_D13	AG31	Configurable	GPIO Expansion 0 IO[13]
J10-20	GPIO0_D14	AF32	Configurable	GPIO Expansion 0 IO[14]
J10-22	GPIO0_D15	AF31	Configurable	GPIO Expansion 0 IO[15]
J10-23	GPIO0_D16	AP21	Configurable	GPIO Expansion 0 IO[16]
J10-24	GPIO0_D17	AG34	Configurable	GPIO Expansion 0 IO[17]
J10-25	GPIO0_D18	AN21	Configurable	GPIO Expansion 0 IO[18]
J10-26	GPIO0_D19	AH33	Configurable	GPIO Expansion 0 IO[19]
J10-27	GPIO0_D20	AL21	Configurable	GPIO Expansion 0 IO[20]
J10-28	GPIO0_D21	AP22	Configurable	GPIO Expansion 0 IO[21]
J10-31	GPIO0_D22	AK21	Configurable	GPIO Expansion 0 IO[22]
J10-32	GPIO0_D23	AN22	Configurable	GPIO Expansion 0 IO[23]
J10-33	GPIO0_D24	AP25	Configurable	GPIO Expansion 0 IO[24]
J10-34	GPIO0_D25	AP24	Configurable	GPIO Expansion 0 IO[25]
J10-35	GPIO0_D26	AN25	Configurable	GPIO Expansion 0 IO[26]

J10-36	GPIO0_D27	AN24	Configurable	GPIO Expansion 0 IO[27]
J10-37	GPIO0_D28	AM23	Configurable	GPIO Expansion 0 IO[28]
J10-38	GPIO0_D29	AG21	Configurable	GPIO Expansion 0 IO[29]
J10-39	GPIO0_D30	AL23	Configurable	GPIO Expansion 0 IO[30]
J10-40	GPIO0_D31	AF21	Configurable	GPIO Expansion 0 IO[31]

Table A-13 GPIO Expansion Header 1 pinout with FPGA

Board Reference	Signal Name	FPGA Pin No.	I/O Standard	Description
J11-1	GPIO_CLKINn1	AP19	Configurable	GPIO Expansion 1 Clock In
J11-3	GPIO_CLKINp1	AN19	Configurable	GPIO Expansion 1 Clock In
J11-19	GPIO_CLKOUTn1	AE18	Configurable	GPIO Expansion 1 PLL Out
J11-21	GPIO_CLKOUTp1	AD18	Configurable	GPIO Expansion 1 PLL Out
J11-2	GPIO1_D0	AC26	Configurable	GPIO Expansion 1 IO[0]
J11-4	GPIO1_D1	AC25	Configurable	GPIO Expansion 1 IO[1]
J11-5	GPIO1_D2	AE28	Configurable	GPIO Expansion 1 IO[2]
J11-6	GPIO1_D3	AD27	Configurable	GPIO Expansion 1 IO[3]
J11-7	GPIO1_D4	AF27	Configurable	GPIO Expansion 1 IO[4]
J11-8	GPIO1_D5	AD26	Configurable	GPIO Expansion 1 IO[5]
J11-9	GPIO1_D6	AD29	Configurable	GPIO Expansion 1 IO[6]
J11-10	GPIO1_D7	AF29	Configurable	GPIO Expansion 1 IO[7]
J11-13	GPIO1_D8	AD28	Configurable	GPIO Expansion 1 IO[8]
J11-14	GPIO1_D9	AF28	Configurable	GPIO Expansion 1 IO[9]
J11-15	GPIO1_D10	AB27	Configurable	GPIO Expansion 1 IO[10]
J11-16	GPIO1_D11	AE30	Configurable	GPIO Expansion 1 IO[11]
J11-17	GPIO1_D12	AB26	Configurable	GPIO Expansion 1 IO[12]
J11-18	GPIO1_D13	AE29	Configurable	GPIO Expansion 1 IO[13]
J11-20	GPIO1_D14	AB25	Configurable	GPIO Expansion 1 IO[14]
J11-22	GPIO1_D15	AB24	Configurable	GPIO Expansion 1 IO[15]
J11-23	GPIO1_D16	AM21	Configurable	GPIO Expansion 1 IO[16]
J11-24	GPIO1_D17	AD31	Configurable	GPIO Expansion 1 IO[17]
J11-25	GPIO1_D18	AP20	Configurable	GPIO Expansion 1 IO[18]
J11-26	GPIO1_D19	AD30	Configurable	GPIO Expansion 1 IO[19]
J11-27	GPIO1_D20	AL22	Configurable	GPIO Expansion 1 IO[20]
J11-28	GPIO1_D21	AJ20	Configurable	GPIO Expansion 1 IO[21]
J11-31	GPIO1_D22	AM22	Configurable	GPIO Expansion 1 IO[22]

J11-32	GPIO1_D23	AJ21	Configurable	GPIO Expansion 1 IO[23]
J11-33	GPIO1_D24	AD21	Configurable	GPIO Expansion 1 IO[24]
J11-34	GPIO1_D25	AP26	Configurable	GPIO Expansion 1 IO[25]
J11-35	GPIO1_D26	AE20	Configurable	GPIO Expansion 1 IO[26]
J11-36	GPIO1_D27	AP23	Configurable	GPIO Expansion 1 IO[27]
J11-37	GPIO1_D28	AK24	Configurable	GPIO Expansion 1 IO[28]
J11-38	GPIO1_D29	AE22	Configurable	GPIO Expansion 1 IO[29]
J11-39	GPIO1_D30	AL25	Configurable	GPIO Expansion 1 IO[30]
J11-40	GPIO1_D31	AE21	Configurable	GPIO Expansion 1 IO[31]

■ DDR2 SO-DIMM Socket

Table A-14 DDR2 SO-DIMM socket pinout with FPGA

Board Reference	Signal Name	FPGA Pin No.	I/O Standard	Description
J9-114	DDR2_ODT0	AM15	SSTL-18 Class I	DDR2 On Die Termination[0]
J9-119	DDR2_ODT1	AJ16	SSTL-18 Class I	DDR2 On Die Termination[1]
J9-30	DDR2_CLK_p0	AE4	SSTL-18 Class I	Clock p0 for DDR2
J9-32	DDR2_CLK_n0	AE3	SSTL-18 Class I	Clock n0 for DDR2
J9-164	DDR2_CLK_p1	AE11	SSTL-18 Class I	Clock p1 for DDR2
J9-166	DDR2_CLK_n1	AF11	SSTL-18 Class I	Clock n1 for DDR2
J9-79	DDR2_CKE0	AF6	SSTL-18 Class I	Clock Enable pin 0 for DDR2
J9-80	DDR2_CKE1	AC11	SSTL-18 Class I	Clock Enable pin 1 for DDR2
J9-5	DDR2_DQ0	AM1	SSTL-18 Class I	DDR2 Data [0]
J9-7	DDR2_DQ1	AM2	SSTL-18 Class I	DDR2 Data [1]
J9-17	DDR2_DQ2	AL1	SSTL-18 Class I	DDR2 Data [2]
J9-19	DDR2_DQ3	AL2	SSTL-18 Class I	DDR2 Data [3]
J9-4	DDR2_DQ4	AE7	SSTL-18 Class I	DDR2 Data [4]
J9-6	DDR2_DQ5	AE8	SSTL-18 Class I	DDR2 Data [5]
J9-14	DDR2_DQ6	AC8	SSTL-18 Class I	DDR2 Data [6]
J9-16	DDR2_DQ7	AC9	SSTL-18 Class I	DDR2 Data [7]
J9-23	DDR2_DQ8	AG3	SSTL-18 Class I	DDR2 Data [8]
J9-25	DDR2_DQ9	AG4	SSTL-18 Class I	DDR2 Data [9]
J9-35	DDR2_DQ10	AJ1	SSTL-18 Class I	DDR2 Data [10]
J9-37	DDR2_DQ11	AH2	SSTL-18 Class I	DDR2 Data [11]
J9-20	DDR2_DQ12	AE5	SSTL-18 Class I	DDR2 Data [12]

J9-22	DDR2_DQ13	AE6	SSTL-18 Class I	DDR2 Data [13]
J9-36	DDR2_DQ14	AD6	SSTL-18 Class I	DDR2 Data [14]
J9-38	DDR2_DQ15	AD7	SSTL-18 Class I	DDR2 Data [15]
J9-43	DDR2_DQ16	AF3	SSTL-18 Class I	DDR2 Data [16]
J9-45	DDR2_DQ17	AF4	SSTL-18 Class I	DDR2 Data [17]
J9-55	DDR2_DQ18	AF1	SSTL-18 Class I	DDR2 Data [18]
J9-57	DDR2_DQ19	AF2	SSTL-18 Class I	DDR2 Data [19]
J9-44	DDR2_DQ20	AC7	SSTL-18 Class I	DDR2 Data [20]
J9-46	DDR2_DQ21	AB8	SSTL-18 Class I	DDR2 Data [21]
J9-56	DDR2_DQ22	AC5	SSTL-18 Class I	DDR2 Data [22]
J9-58	DDR2_DQ23	AC6	SSTL-18 Class I	DDR2 Data [23]
J9-61	DDR2_DQ24	AJ15	SSTL-18 Class I	DDR2 Data [24]
J9-63	DDR2_DQ25	AH15	SSTL-18 Class I	DDR2 Data [25]
J9-73	DDR2_DQ26	AP12	SSTL-18 Class I	DDR2 Data [26]
J9-75	DDR2_DQ27	AN12	SSTL-18 Class I	DDR2 Data [27]
J9-62	DDR2_DQ28	AK15	SSTL-18 Class I	DDR2 Data [28]
J9-64	DDR2_DQ29	AG15	SSTL-18 Class I	DDR2 Data [29]
J9-74	DDR2_DQ30	AP13	SSTL-18 Class I	DDR2 Data [30]
J9-76	DDR2_DQ31	AM12	SSTL-18 Class I	DDR2 Data [31]
J9-123	DDR2_DQ32	AP10	SSTL-18 Class I	DDR2 Data [32]
J9-125	DDR2_DQ33	AN10	SSTL-18 Class I	DDR2 Data [33]
J9-135	DDR2_DQ34	AF14	SSTL-18 Class I	DDR2 Data [34]
J9-137	DDR2_DQ35	AF13	SSTL-18 Class I	DDR2 Data [35]
J9-124	DDR2_DQ36	AP11	SSTL-18 Class I	DDR2 Data [36]
J9-126	DDR2_DQ37	AP9	SSTL-18 Class I	DDR2 Data [37]
J9-134	DDR2_DQ38	AE14	SSTL-18 Class I	DDR2 Data [38]
J9-136	DDR2_DQ39	AE13	SSTL-18 Class I	DDR2 Data [39]
J9-141	DDR2_DQ40	AL12	SSTL-18 Class I	DDR2 Data [40]
J9-143	DDR2_DQ41	AK12	SSTL-18 Class I	DDR2 Data [41]
J9-151	DDR2_DQ42	AP7	SSTL-18 Class I	DDR2 Data [42]
J9-153	DDR2_DQ43	AN7	SSTL-18 Class I	DDR2 Data [43]
J9-140	DDR2_DQ44	AM11	SSTL-18 Class I	DDR2 Data [44]
J9-142	DDR2_DQ45	AK10	SSTL-18 Class I	DDR2 Data [45]
J9-152	DDR2_DQ46	AM7	SSTL-18 Class I	DDR2 Data [46]
J9-154	DDR2_DQ47	AP6	SSTL-18 Class I	DDR2 Data [47]
J9-157	DDR2_DQ48	AJ12	SSTL-18 Class I	DDR2 Data [48]
J9-159	DDR2_DQ49	AH12	SSTL-18 Class I	DDR2 Data [49]

J9-173	DDR2_DQ50	AL9	SSTL-18 Class I	DDR2 Data [50]
J9-175	DDR2_DQ51	AK9	SSTL-18 Class I	DDR2 Data [51]
J9-158	DDR2_DQ52	AJ13	SSTL-18 Class I	DDR2 Data [52]
J9-160	DDR2_DQ53	AG12	SSTL-18 Class I	DDR2 Data [53]
J9-174	DDR2_DQ54	AJ9	SSTL-18 Class I	DDR2 Data [54]
J9-176	DDR2_DQ55	AL7	SSTL-18 Class I	DDR2 Data [55]
J9-179	DDR2_DQ56	AP4	SSTL-18 Class I	DDR2 Data [56]
J9-181	DDR2_DQ57	AN4	SSTL-18 Class I	DDR2 Data [57]
J9-189	DDR2_DQ58	AM5	SSTL-18 Class I	DDR2 Data [58]
J9-191	DDR2_DQ59	AL5	SSTL-18 Class I	DDR2 Data [59]
J9-180	DDR2_DQ60	AP5	SSTL-18 Class I	DDR2 Data [60]
J9-182	DDR2_DQ61	AP2	SSTL-18 Class I	DDR2 Data [61]
J9-192	DDR2_DQ62	AM4	SSTL-18 Class I	DDR2 Data [62]
J9-194	DDR2_DQ63	AL4	SSTL-18 Class I	DDR2 Data [63]
J9-107	DDR2_BA0	AM17	SSTL-18 Class I	DDR2 Bank Address [0]
J9-106	DDR2_BA1	AE12	SSTL-18 Class I	DDR2 Bank Address [1]
J9-85	DDR2_BA2	AP14	SSTL-18 Class I	DDR2 Bank Address [2]
J9-102	DDR2_A0	AE10	SSTL-18 Class I	DDR2 Address [0]
J9-101	DDR2_A1	AD12	SSTL-18 Class I	DDR2 Address [1]
J9-100	DDR2_A2	AF10	SSTL-18 Class I	DDR2 Address [2]
J9-99	DDR2_A3	AL14	SSTL-18 Class I	DDR2 Address [3]
J9-98	DDR2_A4	AJ6	SSTL-18 Class I	DDR2 Address [4]
J9-97	DDR2_A5	AM14	SSTL-18 Class I	DDR2 Address [5]
J9-94	DDR2_A6	AK6	SSTL-18 Class I	DDR2 Address [6]
J9-92	DDR2_A7	AM6	SSTL-18 Class I	DDR2 Address [7]
J9-93	DDR2_A8	AJ7	SSTL-18 Class I	DDR2 Address [8]
J9-91	DDR2_A9	AK7	SSTL-18 Class I	DDR2 Address [9]
J9-105	DDR2_A10	AC12	SSTL-18 Class I	DDR2 Address [10]
J9-90	DDR2_A11	AJ10	SSTL-18 Class I	DDR2 Address [11]
J9-89	DDR2_A12	AM8	SSTL-18 Class I	DDR2 Address [12]
J9-116	DDR2_A13	AL15	SSTL-18 Class I	DDR2 Address [13]
J9-86	DDR2_A14	AE15	SSTL-18 Class I	DDR2 Address [14]
J9-84	DDR2_A15	AA10	SSTL-18 Class I	DDR2 Address [15]
J9-11	DDR2_DQSn0	AJ3	SSTL-18 Class I	DDR2 Data Strobe n[0]
J9-13	DDR2_DQSp0	AJ4	SSTL-18 Class I	DDR2 Data Strobe p[0]
J9-29	DDR2_DQSn1	AK1	SSTL-18 Class I	DDR2 Data Strobe n[1]
J9-31	DDR2_DQSp1	AJ2	SSTL-18 Class I	DDR2 Data Strobe p[1]

J9-49	DDR2_DQSn2	AH1	SSTL-18 Class I	DDR2 Data Strobe n[2]
J9-51	DDR2_DQSp2	AG1	SSTL-18 Class I	DDR2 Data Strobe p[2]
J9-68	DDR2_DQSn3	AJ14	SSTL-18 Class I	DDR2 Data Strobe n[3]
J9-70	DDR2_DQSp3	AH14	SSTL-18 Class I	DDR2 Data Strobe p[3]
J9-129	DDR2_DQSn4	AN9	SSTL-18 Class I	DDR2 Data Strobe n[4]
J9-131	DDR2_DQSp4	AM9	SSTL-18 Class I	DDR2 Data Strobe p[4]
J9-146	DDR2_DQSn5	AL11	SSTL-18 Class I	DDR2 Data Strobe n[5]
J9-148	DDR2_DQSp5	AL10	SSTL-18 Class I	DDR2 Data Strobe p[5]
J9-167	DDR2_DQSn6	AJ11	SSTL-18 Class I	DDR2 Data Strobe n[6]
J9-169	DDR2_DQSp6	AH11	SSTL-18 Class I	DDR2 Data Strobe p[6]
J9-186	DDR2_DQSn7	AP3	SSTL-18 Class I	DDR2 Data Strobe n[7]
J9-188	DDR2_DQSp7	AN3	SSTL-18 Class I	DDR2 Data Strobe p[7]
J9-10	DDR2_DM0	AF5	SSTL-18 Class I	DDR2 Data Mask [0]
J9-26	DDR2_DM1	AB10	SSTL-18 Class I	DDR2 Data Mask [1]
J9-52	DDR2_DM2	AB9	SSTL-18 Class I	DDR2 Data Mask [2]
J9-67	DDR2_DM3	AN13	SSTL-18 Class I	DDR2 Data Mask [3]
J9-130	DDR2_DM4	AF15	SSTL-18 Class I	DDR2 Data Mask [4]
J9-147	DDR2_DM5	AP8	SSTL-18 Class I	DDR2 Data Mask [5]
J9-170	DDR2_DM6	AL8	SSTL-18 Class I	DDR2 Data Mask [6]
J9-185	DDR2_DM7	AN6	SSTL-18 Class I	DDR2 Data Mask [7]
J9-108	DDR2_RAS_n	AL13	SSTL-18 Class I	DDR2 Row Address Strobe
J9-113	DDR2_CAS_n	AD13	SSTL-18 Class I	DDR2 Column Address Strobe
J9-109	DDR2_WE_n	AL17	SSTL-18 Class I	DDR2 Write Enable
J9-110	DDR2_CS_n0	AM16	SSTL-18 Class I	DDR2 Chip Select [0]
J9-115	DDR2_CS_n1	AL16	SSTL-18 Class I	DDR2 Chip Select [1]
J9-198	DDR2_SA0	U6	3.3V	DDR2 Presence-detect address input [0]
J9-200	DDR2_SA1	T7	3.3V	DDR2 Presence-detect address input [1]
J9-197	DDR2_SCL	T8	3.3V	DDR2 I2C Clock
J9-195	DDR2_SDA	T9	3.3V	DDR2 I2C Data

■ USB Host/Device Controller

Table A-15 The USB2.0 OTG pinout with FPGA				
Board Reference	Signal Name	FPGA Pin No.	I/O Standard	Description
U2-H16	OTG_A1	N32	3.3V	OTG Address [1]
U2-H15	OTG_A2	L34	3.3V	OTG Address [2]
U2-H14	OTG_A3	M31	3.3V	OTG Address [3]
U2-F16	OTG_A4	N33	3.3V	OTG Address [4]
U2-F15	OTG_A5	M33	3.3V	OTG Address [5]
U2-F14	OTG_A6	M34	3.3V	OTG Address [6]
U2-E15	OTG_A7	N34	3.3V	OTG Address [7]
U2-D16	OTG_A8	N31	3.3V	OTG Address [8]
U2-C16	OTG_A9	P34	3.3V	OTG Address [9]
U2-C15	OTG_A10	P31	3.3V	OTG Address [10]
U2-B16	OTG_A11	P32	3.3V	OTG Address [11]
U2-B15	OTG_A12	R34	3.3V	OTG Address [12]
U2-A15	OTG_A13	R33	3.3V	OTG Address [13]
U2-B14	OTG_A14	R32	3.3V	OTG Address [14]
U2-A14	OTG_A15	T32	3.3V	OTG Address [15]
U2-A13	OTG_A16	U32	3.3V	OTG Address [16]
U2-C12	OTG_A17	R31	3.3V	OTG Address [17]
U2-R3	OTG_D0	Y25	3.3V	OTG Data [0]
U2-T3	OTG_D1	AA27	3.3V	OTG Data [1]
U2-R4	OTG_D2	Y26	3.3V	OTG Data [2]
U2-P5	OTG_D3	AA30	3.3V	OTG Data [3]
U2-T5	OTG_D4	AB29	3.3V	OTG Data [4]
U2-R5	OTG_D5	AA28	3.3V	OTG Data [5]
U2-R6	OTG_D6	Y31	3.3V	OTG Data [6]
U2-P7	OTG_D7	AA31	3.3V	OTG Data [7]
U2-T7	OTG_D8	Y32	3.3V	OTG Data [8]
U2-T8	OTG_D9	Y34	3.3V	OTG Data [9]
U2-P9	OTG_D10	AB31	3.3V	OTG Data [10]
U2-T9	OTG_D11	AA32	3.3V	OTG Data [11]
U2-T10	OTG_D12	AA33	3.3V	OTG Data [12]
U2-P11	OTG_D13	AD34	3.3V	OTG Data [13]

U2-T11	OTG_D14	AA34	3.3V	OTG Data [14]
U2-R11	OTG_D15	AC34	3.3V	OTG Data [15]
U2-R12	OTG_D16	AB30	3.3V	OTG Data [16]
U2-T13	OTG_D17	AB33	3.3V	OTG Data [17]
U2-R13	OTG_D18	AD33	3.3V	OTG Data [18]
U2-T14	OTG_D19	AB34	3.3V	OTG Data [19]
U2-T15	OTG_D20	AB32	3.3V	OTG Data [20]
U2-R15	OTG_D21	V24	3.3V	OTG Data [21]
U2-T16	OTG_D22	W26	3.3V	OTG Data [22]
U2-R16	OTG_D23	V25	3.3V	OTG Data [23]
U2-P16	OTG_D24	W30	3.3V	OTG Data [24]
U2-N15	OTG_D25	W27	3.3V	OTG Data [25]
U2-M15	OTG_D26	W31	3.3V	OTG Data [26]
U2-M16	OTG_D27	W24	3.3V	OTG Data [27]
U2-L16	OTG_D28	Y23	3.3V	OTG Data [28]
U2-L15	OTG_D29	Y29	3.3V	OTG Data [29]
U2-K16	OTG_D30	Y28	3.3V	OTG Data [30]
U2-K14	OTG_D31	AA29	3.3V	OTG Data [31]
U2-A12	OTG_CS_n	P28	3.3V	OTG Chip Select
U2-B11	OTG_WE_n	N29	3.3V	OTG Write Enable
U2-B12	OTG_OE_n	N30	3.3V	OTG Output Enable
U2-B10	OTG_HC_IRQ	P29	3.3V	OTG Host Controller IRQ
U2-A10	OTG_DC_IRQ	R27	3.3V	OTG Peripheral Controller IRQ
U2-B6	OTG_RESET_n	T23	3.3V	OTG Reset
U2-B9	OTG_HC_DREQ	R28	3.3V	OTG DMA Controller request for Host Controller
U2-A8	OTG__HC_DACK	R25	3.3V	OTG DMA Controller request Acknowledgement
U2-A9	OTG_DC_DREQ	R26	3.3V	OTG DMA Controller request for the Peripheral Controller
U2-B8	OTG_DC_DACK	R24	3.3V	Peripheral Controller DMA request acknowledgement
U2-F1	12MHz			OTG CLK input
U2-J1	PSW1			Power Switch for port 1
U2-H1	DM1			Downstream data minus port 1
U2-J2	DP1			Downstream data plus port 1
U2-B2	USB_ID			ID input to detect the default host or peripheral

				setting when port 1 is in OTG mode JP1 : Open ➔ port1 set to peripheral Close ➔ port 1 set to host
U2-M1	PSW2			Power Switch for port 2
U2-L1	DM2			Downstream data minus port 2
U2-M2	DP2			Downstream data plus port 2
U2-T1	PSW3			Power Switch for port 3
U2-P1	DM3			Downstream data minus port 3
U2-R1	DP3			Downstream data plus port 3

■ SD Card Socket

Table A-16 The SD card socket pinout with FPGA

Board Reference	Signal Name	FPGA Pin No.	I/O Standard	Description
J12-5	SD_CLK	P8	3.3V	Clock for SD
J12-11	SD_WPn	N5	3.3V	Write Protection for SD
J12-7	SD_DAT0	P7	3.3V	Data bit 0 for SD
J12-2	SD_CMD	R10	3.3V	Command for SD

■ Clock

Table A-17 The clock pinout with FPGA

Board Reference	Signal Name	FPGA Pin No.	I/O Standard	Description
U19-3	OSC_BA	AN18	Configurable	Clock input for I/O Group A
U19-5	OSC_BB	AN16	Configurable	Clock input for I/O Group B
U19-7	OSC_BC	B17	Configurable	Clock input for I/O Group C
U19-10	OSC_BD	B19	Configurable	Clock input for I/O Group D
U19-12	OSC1_50	T33	3.3V	Clock input for I/O Bank 1
U19-14	OSC2_50	W2	3.3V	Clock input for I/O Bank 5
J10	EXT_CLK	U2	3.3V	External Clock input for I/O Bank 6 from SMA
J11	CLK_OUT	V10	3.3V	PLL clock output to SMA

■ Temperature Sensor

Table A-18 The Temperature Sensor pinout with FPGA				
Board Reference	**Signal Name**	**FPGA Pin No.**	**I/O Standard**	**Description**
U5-3	TEMPDIODEn	D4	3.3V	Negative pin of Temperature Diode in Stratix III
U5-4	TEMPDIODEp	E5	3.3V	Positive pin of Temperature Diode in Stratix III
U5-9	TEMP_OVERn			Overtemperature Alarm
U5-11	TEMP_INTn	N2	3.3V	SMBus Alert (interrupt)
U5-12	TEMP_DATA	P1	3.3V	SMBus Data
U5-14	TEMP_CLK	P4	3.3V	SMBus Clock

Appendix B

Pin Compatible List for HSTC and HSMC Connector

Table B-1 Pin Compatible List for HSTC and HSMC Connectors

HSTC Connector		HSMC Connector		
Pin Number	Signal Name	Pin Number	Signal Name	
			Differential	Single-ended
2	PSNT_n	160	PSNT_n	PSNT_n
3	CLKOUT_n0	157	CLKOUT2n (LVDS CLKn / CMOS)	D78 (LVDS CLKn / CMOS)
4	CLKIN_n0	158	CLKIN2n (LVDS CLKn / CMOS)	D79 (LVDS CLKn / CMOS)
5	CLKOUT_p0	155	CLKOUT2p (LVDS_CLKp / CMOS)	D76 (LVDS_CLKp / CMOS)
6	CLKIN_p0	156	CLKIN2p (LVDS_CLKp / CMOS)	D77 (LVDS_CLKp / CMOS)
9	TX_n0	151	LVDS_TXn16 (LVDS)	D74 (CMOS)
10	RX_n0	152	LVDS_RXn16 (LVDS)	D75 (CMOS)
11	TX_p0	149	LVDS_TXp16 (LVDS)	D72 (CMOS)
12	RX_p0	150	LVDS_RXp16 (LVDS)	D73 (CMOS)
15	TX_n1	145	LVDS_TXn15 (LVDS)	D70 (CMOS)
16	RX_n1	146	LVDS_RXn15 (LVDS)	D71 (CMOS)
17	TX_p1	143	LVDS_TXp15 (LVDS)	D68 (CMOS)
18	RX_p1	144	LVDS_RXp15 (LVDS)	D69 (CMOS)
21	TX_n2	139	LVDS_TXn14 (LVDS)	D66 (CMOS)
22	RX_n2	140	LVDS_RXn14 (LVDS)	D67 (CMOS)
23	TX_p2	137	LVDS_TXp14 (LVDS)	D64 (CMOS)
24	RX_p2	138	LVDS_RXp14 (LVDS)	D65 (CMOS)
27	TX_n3	133	LVDS_TXn13 (LVDS)	D62 (CMOS)
28	RX_n3	134	LVDS_RXn13 (LVDS)	D63 (CMOS)
29	TX_p3	131	LVDS_TXp13 (LVDS)	D60 (CMOS)
30	RX_p3	132	LVDS_RXp13 (LVDS)	D61 (CMOS)
33	TX_n4	127	LVDS_TXn12 (LVDS)	D58 (CMOS)
34	RX_n4	128	LVDS_RXn12 (LVDS)	D59 (CMOS)
35	TX_p4	125	LVDS_TXp12 (LVDS)	D56 (CMOS)
36	RX_p4	126	LVDS_RXp12 (LVDS)	D57 (CMOS)
39	TX_n5	121	LVDS_TXn11 (LVDS)	D54 (CMOS)
40	RX_n5	122	LVDS_RXn11 (LVDS)	D55 (CMOS)

41	TX_p5	119	LVDS_TXp11 （LVDS）	D52 （CMOS）
42	RX_p5	120	LVDS_RXp11 （LVDS）	D53 （CMOS）
45	TX_n6	115	LVDS_TXn10 （LVDS）	D50 （CMOS）
46	RX_n6	116	LVDS_RXn10 （LVDS）	D51 （CMOS）
47	TX_p6	113	LVDS_TXp10 （LVDS）	D48 （CMOS）
48	RX_p6	114	LVDS_RXp10 （LVDS）	D49 （CMOS）
51	TX_n7	109	LVDS_TXn9 （LVDS）	D46 （CMOS）
52	RX_n7	110	LVDS_RXn9 （LVDS）	D47 （CMOS）
53	TX_p7	107	LVDS_TXp9 （LVDS）	D44 （CMOS）
54	RX_p7	108	LVDS_RXp9 （LVDS）	D45 （CMOS）
57	TX_n8	103	LVDS_TXn8 （LVDS）	D42 （CMOS）
58	RX_n8	104	LVDS_RXn8 （LVDS）	D43 （CMOS）
59	TX_p8	101	LVDS_TXp8 （LVDS）	D40 （CMOS）
60	RX_p8	102	LVDS_RXp8 （LVDS）	D41 （CMOS）
63	CLKOUT_n1	97	CLKOUT1n （LVDS CLKn / CMOS）	D38 （LVDS CLKn / CMOS）
64	CLKIN_n1	98	CLKIN1n （LVDS CLKn / CMOS）	D39 （LVDS CLKn / CMOS）
65	CLKOUT_p1	95	CLKOUT1p （LVDS_CLKp / CMOS）	D36 （LVDS_CLKp / CMOS）
66	CLKIN_p1	96	CLKIN1p （LVDS_CLKp / CMOS）	D37 （LVDS_CLKp / CMOS）
69	TX_n9	91	LVDS_TXn7 （LVDS）	D34 （CMOS）
70	RX_n9	92	LVDS_RXn7 （LVDS）	D35 （CMOS）
71	TX_p9	89	LVDS_TXp7 （LVDS）	D32 （CMOS）
72	RX_p9	90	LVDS_RXp7 （LVDS）	D33 （CMOS）
75	TX_n10	85	LVDS_TXn6 （LVDS）	D30 （CMOS）
76	RX_n10	86	LVDS_RXn6 （LVDS）	D31 （CMOS）
77	TX_p10	83	LVDS_TXp6 （LVDS）	D28 （CMOS）
78	RX_p10	84	LVDS_RXp6 （LVDS）	D29 （CMOS）
81	TX_n11	79	LVDS_TXn5 （LVDS）	D26 （CMOS）
82	RX_n11	80	LVDS_RXn5 （LVDS）	D27 （CMOS）
83	TX_p11	77	LVDS_TXp5 （LVDS）	D24 （CMOS）
84	RX_p11	78	LVDS_RXp5 （LVDS）	D25 （CMOS）
87	TX_n12	73	LVDS_TXn4 （LVDS）	D22 （CMOS）
88	RX_n12	74	LVDS_RXn4 （LVDS）	D23 （CMOS）
89	TX_p12	71	LVDS_TXp4 （LVDS）	D20 （CMOS）
90	RX_p12	72	LVDS_RXp4 （LVDS）	D21 （CMOS）
93	TX_n13	67	LVDS_TXn3 （LVDS）	D18 （CMOS）
94	RX_n13	68	LVDS_RXn3 （LVDS）	D19 （CMOS）
95	TX_p13	65	LVDS_TXp3 （LVDS）	D16 （CMOS）
96	RX_p13	66	LVDS_RXp3 （LVDS）	D17 （CMOS）
99	TX_n14	61	LVDS_TXn2 （LVDS）	D14 （CMOS）
100	RX_n14	62	LVDS_RXn2 （LVDS）	D15 （CMOS）

101	TX_p14	59	LVDS_TXp2 (LVDS)	D12 (CMOS)
102	RX_p14	60	LVDS_RXp2 (LVDS)	D13 (CMOS)
105	TX_n15	55	LVDS_TXn1 (LVDS)	D10 (CMOS)
106	RX_n15	56	LVDS_RXn1 (LVDS)	D11 (CMOS)
107	TX_p15	53	LVDS_TXp1 (LVDS)	D8 (CMOS)
108	RX_p15	54	LVDS_RXp1 (LVDS)	D9 (CMOS)
111	TX_n16	49	LVDS_TXn0 (LVDS)	D6 (CMOS)
112	RX_n16	50	LVDS_RXn0 (LVDS)	D7 (CMOS)
113	TX_p16	47	LVDS_TXp0 (LVDS)	D4 (CMOS)
114	RX_p16	48	LVDS_RXp0 (LVDS)	D5 (CMOS)
117	TX_n17	43	D2 (CMOS)	D2 (CMOS)
118	RX_n17	44	D3 (CMOS)	D3 (CMOS)
119	TX_p17	41	D0 (CMOS)	D0 (CMOS)
120	RX_p17	42	D1 (CMOS)	D1 (CMOS)
121	POWER_ON			
123	CLKOUT_2	39	CLKOUT0 (CMOS CLK)	CLKOUT0 (CMOS CLK)
124	CLKIN_2	40	CLKIN0 (CMOS CLK)	CLKIN0 (CMOS CLK)
125	TDO	37	JTAG_TDO (JTAG / CMOS)	JTAG_TDO (JTAG / CMOS)
126	TDI	38	JTAG_TDI (JTAG / CMOS)	JTAG_TDI (JTAG / CMOS)
129	TCK	35	JTAG_TCK (JTAG / CMOS)	JTAG_TCK (JTAG / CMOS)
130	TMS	36	JTAG_TMS (JTAG / CMOS)	JTAG_TMS (JTAG / CMOS)
131	SDA	33	SDA (SMBUS / CMOS)	SDA (SMBUS / CMOS)
132	SCL	34	SCL (SMBUS / CMOS)	SCL (SMBUS / CMOS)
133	TX_n18			
134	RX_n18			
135	TX_p18	31	TXVR_TXn0 (Transceiver)	D110 (CMOS)
136	RX_p18	32	TXVR_RXn0 (Transceiver)	D111 (CMOS)
137	TX_n19	29	TXVR_TXp0 (Transceiver)	D108 (CMOS)
138	RX_n19	30	TXVR_RXp0 (Transceiver)	D109 (CMOS)
139	TX_p19			
140	RX_p19			
141	TX_n20	27	TXVR_TXn1 (Transceiver)	D106 (CMOS)
142	RX_n20	28	TXVR_RXn1 (Transceiver)	D107 (CMOS)
143	TX_p20	25	TXVR_TXp1 (Transceiver)	D104 (CMOS)
144	RX_p20	26	TXVR_RXp1 (Transceiver)	D105 (CMOS)
145	TX_n21			
146	RX_n21			
147	TX_p21	23	TXVR_TXn2 (Transceiver)	D102 (CMOS)
148	RX_p21	24	TXVR_RXn2 (Transceiver)	D103 (CMOS)
149	TX_n22	21	TXVR_TXp2 (Transceiver)	D100 (CMOS)

150	RX_n22	22	TXVR_RXp2 (Transceiver)	D101 (CMOS)
151	TX_p22			
152	RX_p22			
153	TX_n23	19	TXVR_TXn3 (Transceiver)	D98 (CMOS)
154	RX_n23	20	TXVR_RXn3 (Transceiver)	D99 (CMOS)
155	TX_p23	17	TXVR_TXp3 (Transceiver)	D96 (CMOS)
156	RX_p23	18	TXVR_RXp3 (Transceiver)	D97 (CMOS)
157	TX_n24			
158	RX_n24			
159	TX_p24	15	TXVR_TXn4 (Transceiver)	D94 (CMOS)
160	RX_p24	16	TXVR_RXn4 (Transceiver)	D95 (CMOS)
161	TX_n25	13	TXVR_TXp4 (Transceiver)	D92 (CMOS)
162	RX_n25	14	TXVR_RXp4 (Transceiver)	D91 (CMOS)
163	TX_p25			
164	RX_p25			
165	TX_n26	11	TXVR_TXn5 (Transceiver)	D90 (CMOS)
166	RX_n26	12	TXVR_RXn5 (Transceiver)	D91 (CMOS)
167	TX_p26	9	TXVR_TXp5 (Transceiver)	D88 (CMOS)
168	RX_p26	10	TXVR_RXp5 (Transceiver)	D89 (CMOS)
169	TX_n27			
170	RX_n27			
171	TX_p27	7	TXVR_TXn6 (Transceiver)	D86 (CMOS)
172	RX_p27	8	TXVR_RXn6 (Transceiver)	D87 (CMOS)
173	TX_n28	5	TXVR_TXp6 (Transceiver)	D84 (CMOS)
174	RX_n28	6	TXVR_RXp6 (Transceiver)	D85 (CMOS)
175	TX_p28			
176	RX_p28			
177	TX_n29	3	TXVR_TXn7 (Transceiver)	D82 (CMOS)
178	RX_n29	4	TXVR_RXn7 (Transceiver)	D83 (CMOS)
179	TX_p29	1	TXVR_TXp7 (Transceiver)	D81 (CMOS)
180	RX_p29	2	TXVR_RXp7 (Transceiver)	D80 (CMOS)

Appendix C
Programming the Serial Configuration Device

This appendix describes how to program the serial configuration device with Serial Flash Loader (SFL) function via the JTAG interface. User can program serial configuration devices with a JTAG indirect configuration (.jic) file. To generate JIC programming files with the Quartus II software, users need to generate a user-specified SRAM object file (.sof), which is the input file first. Next, users need to convert the SOF to a JIC file. To convert a SOF to a JIC file in Quartus II software, follow these steps:

■ Convert SOF to JIC

1. Choose **Convert Programming Files** (File menu).
2. In the **Convert Programming Files** dialog box, scroll to the **JTAG Indirect Configuration File** (.jic) from the **Programming file type** field.
3. In the **Configuration device** field, specify the targeted serial configuration device (For DE3-340 and DE3-260 please select EPCS128. For DE3-150 please select EPCS64).
4. In the **File name** field, browse to the target directory and specify an output file name.
5. Highlight the SOF data in the Input files to convert section. See Figure C.1.
6. Click **Add File**.
7. Select the SOF that you want to convert to a JIC file.
8. Click **Open**.
9. Highlight the Flash Loader and click **Add Device**. See Figure C.2.
10. Click **OK**. The Select Devices page displays.

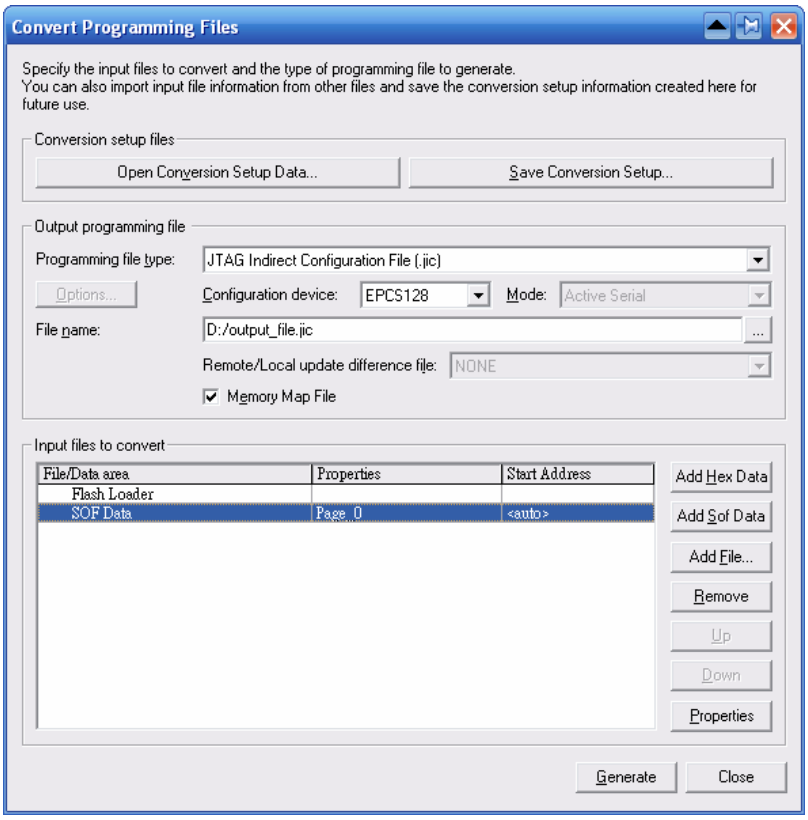


Figure C.1. Convert Programming Files Dialog Box

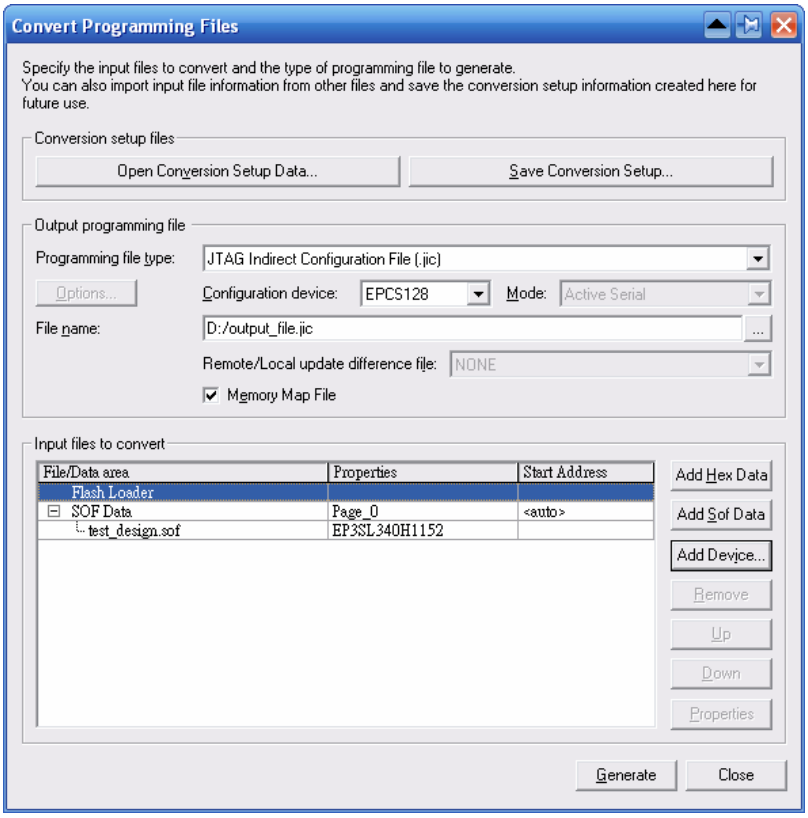


Figure C.2. Highlight Flash Loader

11. Select the targeted FPGA that you are using to program the serial configuration device. See Figure C.3.

12. Click OK. The **Convert Programming Files** page displays. See Figure C.4.

13. Click **Generate**.

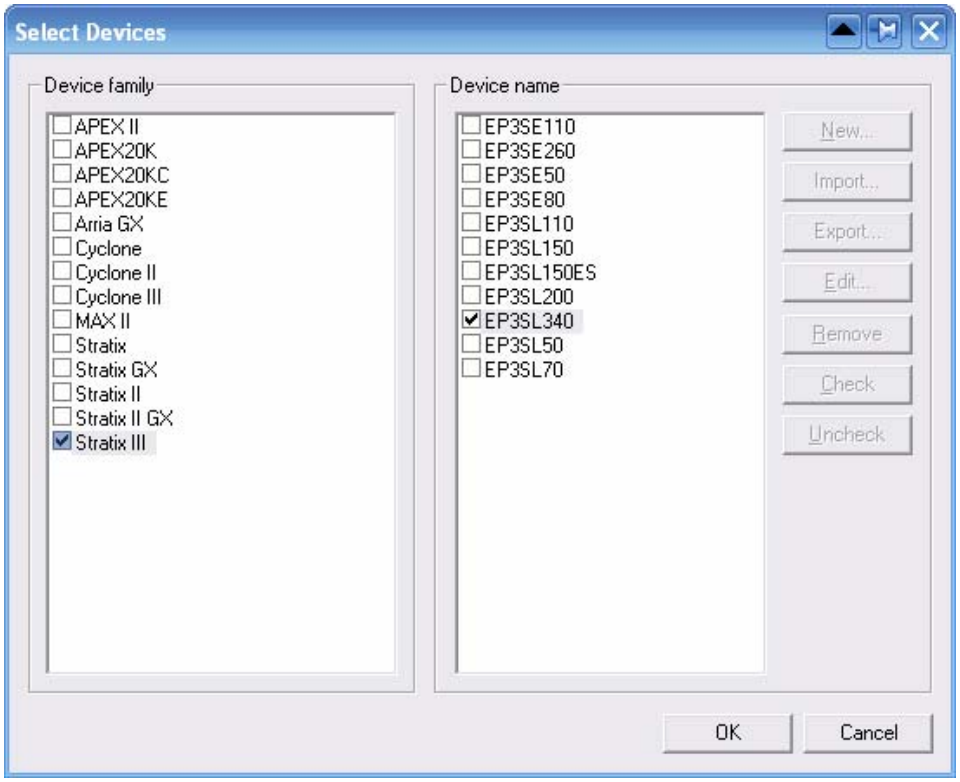


Figure C.3. Select Devices Page

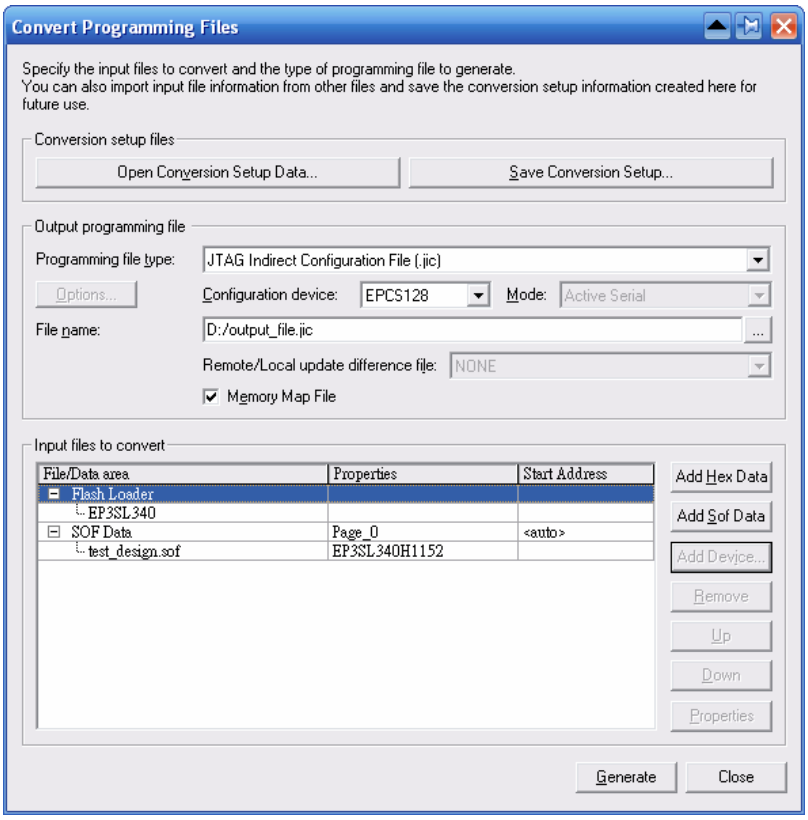


Figure C.4. Convert Programming Files Page

■ Write JIC File into Serial Configuration Device

To program the serial configuration device with the JIC file that you just created, add the file to the Quartus II Programmer window and follow the steps:

1. When the SOF-to-JIC file conversion is complete, add the JIC file to the Quartus II Programmer window:
   i. Choose **Programmer** (Tools menu). The **Chain1.cdf** window displays.
   ii. Click **Add File**. From the **Select Programming File** page, browse to the JIC file.
   iii. Click **Open**.

2. Program the serial configuration device by checking the corresponding **Program/Configure** box, a Factory default SFL image will be load (See Figure C.5).

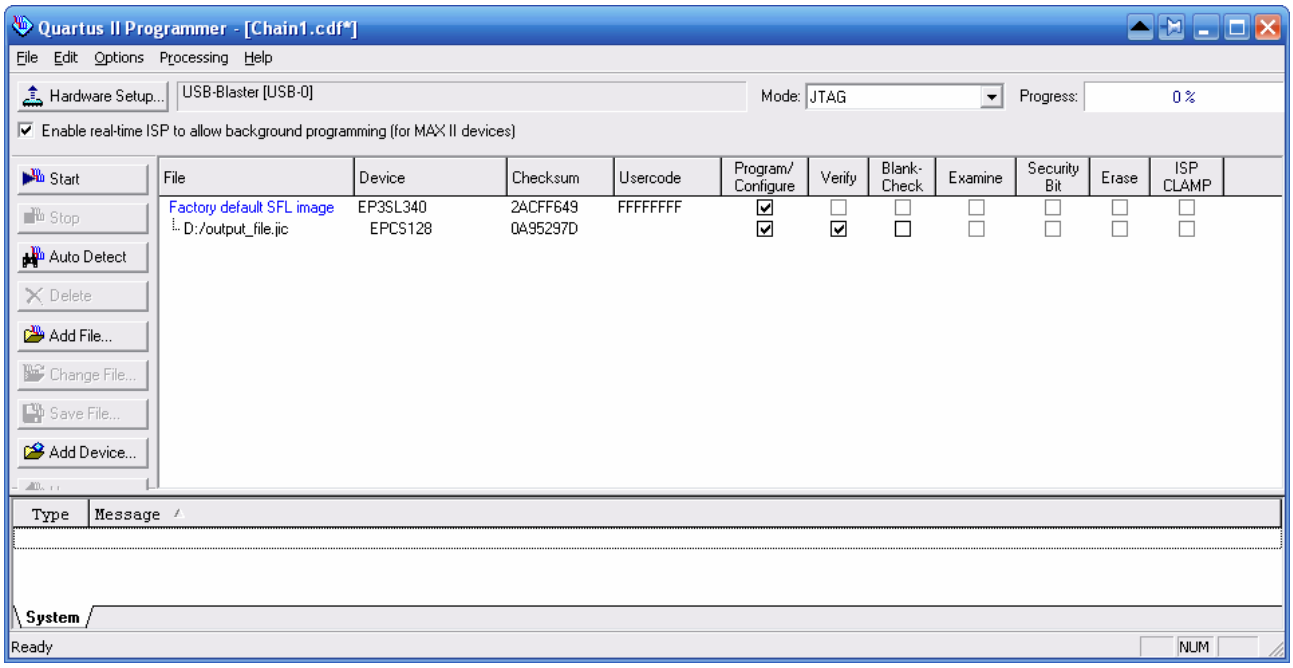


Figure C.5. Quartus II programmer window with one JIC file

3. Click **Start** to program serial configuration device.

■ Erase the Serial Configuration Device

To erase the existed file in the serial configuration device, follow the steps listed below:

1. Choose **Programmer** (Tools menu). The **Chain1.cdf** window displays.

2. Click **Add File**. From the Select Programming File page, browse to a JIC file.

3. Click **Open.**

4. Erase the serial configuration device by checking the corresponding **Erase** box, a Factory default SFL image will be load (See Figure C.6).

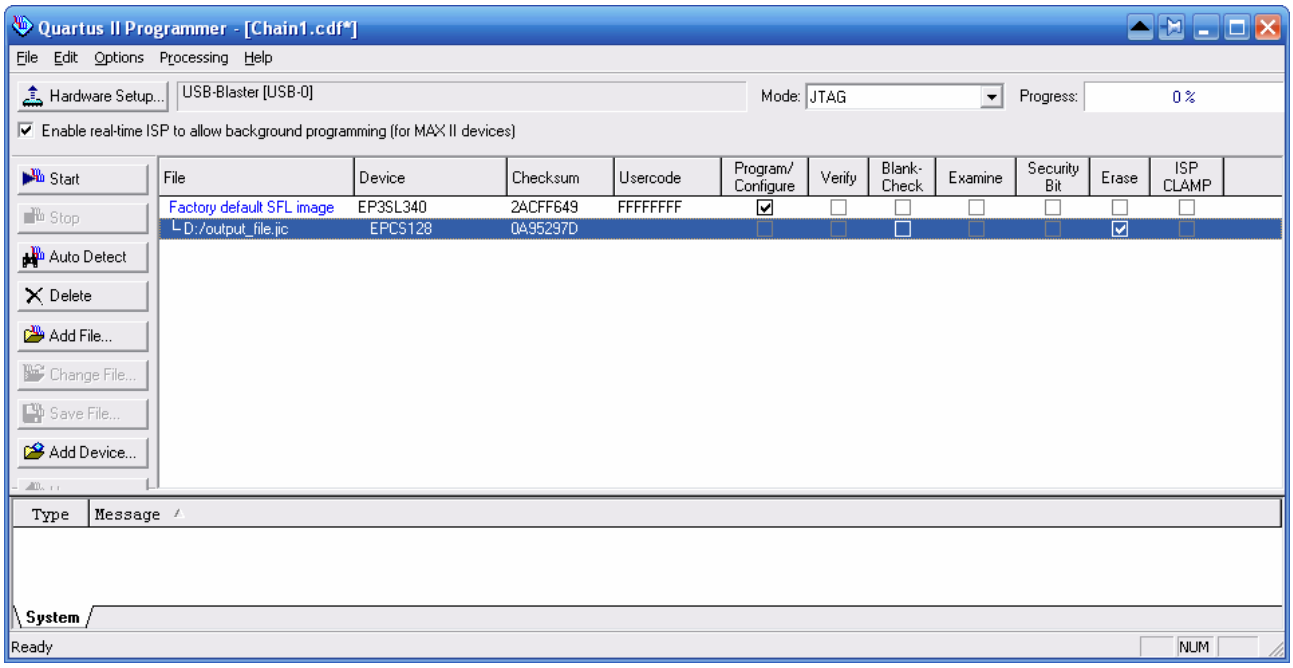


Figure C.6 Erasing setting in Quartus II programmer window

5. Click **Start** to erase the serial configuration device.

Appendix D
DE3_HSTC Utility

DE3_HSTC utility is to test the connection between I/O pins of HSTC connectors and Stratix III FPGA on DE3 board. To perform this test, a THDB_HLB adapter card as shown in Figure D.1will be used which can be found in the DE3 package. The detailed test procedures are list in below:

1. Copy the whole folder named "**DE3_HSTC_Loopback**" from the **DE3_System_CD** to the host computer.

2. Execute the "**DE3_HSTC.exe**" in the "**DE3_HSTC_Loopback**" folder.

3. Make sure the power of the DE3 board is turned off and all the daughter boards are removed from DE3 board.

4. Connect the THDB_HLB adapter card to the HSTC connector which is needed to be tested as shown in Figure D.2.

5. Turn on the power of the DE3 board and connect the USB cable to the USB-Blaster port on the DE3 board.

6. In the **DE3_HSTC** utility window, press "**Test HSTC-A**" button to start testing the HSTC connector A as shown in Figure D.3.

7. The test result will be reported on the panel of the DE3_HSTC utility as shown in Figure D.4.

8. If the test result is failed, the HSTC pin number of the invalid pins will be listed on the panel of the DE3_HSTC utility as shown in Figure D.5.

9. To test the rest of the HSCT connectors, connect the TRDB_HLB adapter card to the other HSTC connector and redo the steps 3 to 8.

10. Finally, the HSTC connectors (J2, J4, J6, and J8) on the bottom side of the DE3 board also can use this utility and THDB_HLB card to perform the connection test.

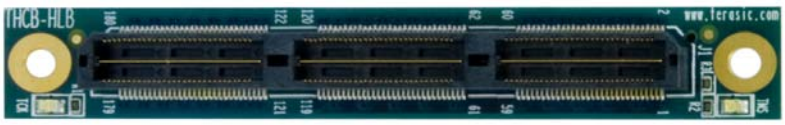


Figure D.1. The THDB_HLB adapter card

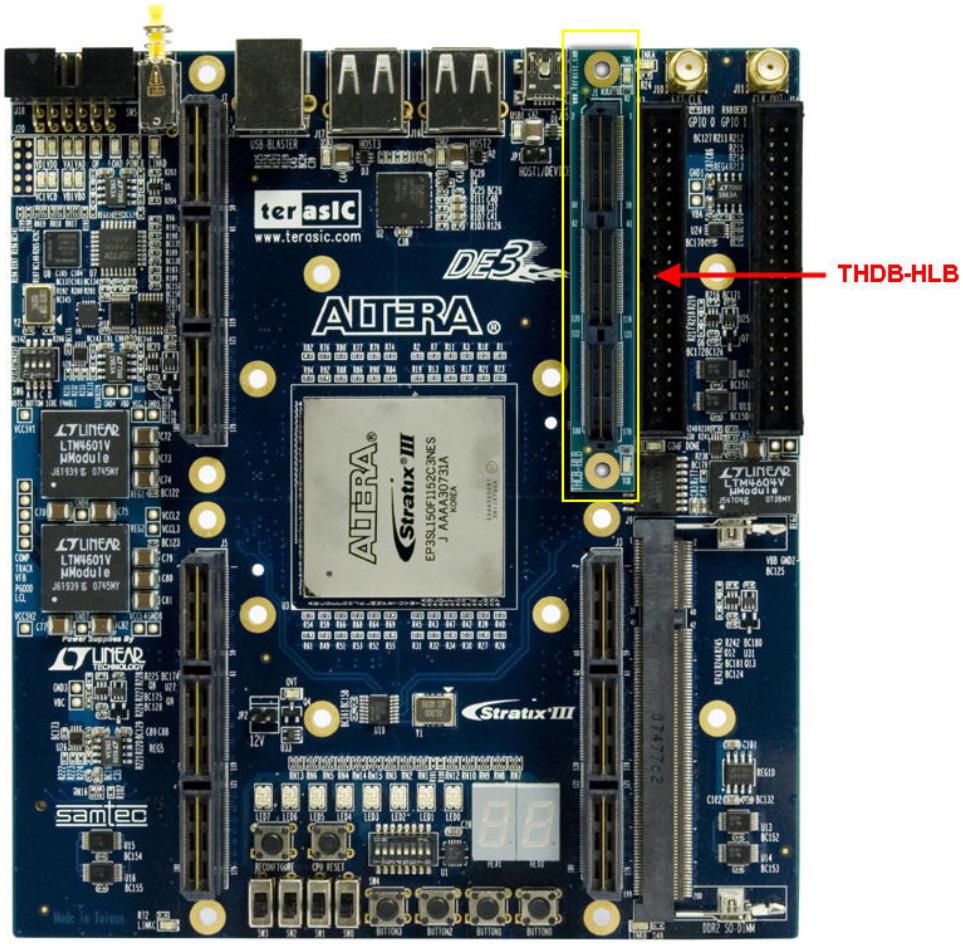


Figure D.2. The connection setup for THDB-HLB and DE3 board

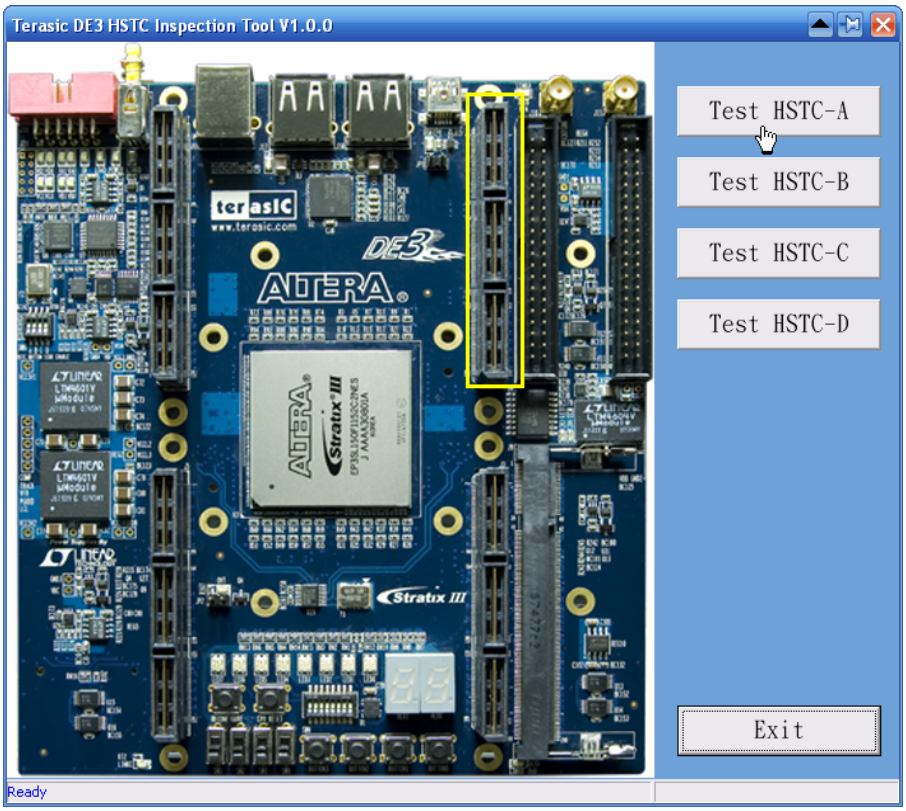


Figure D.3. The DE3_HSTC utility

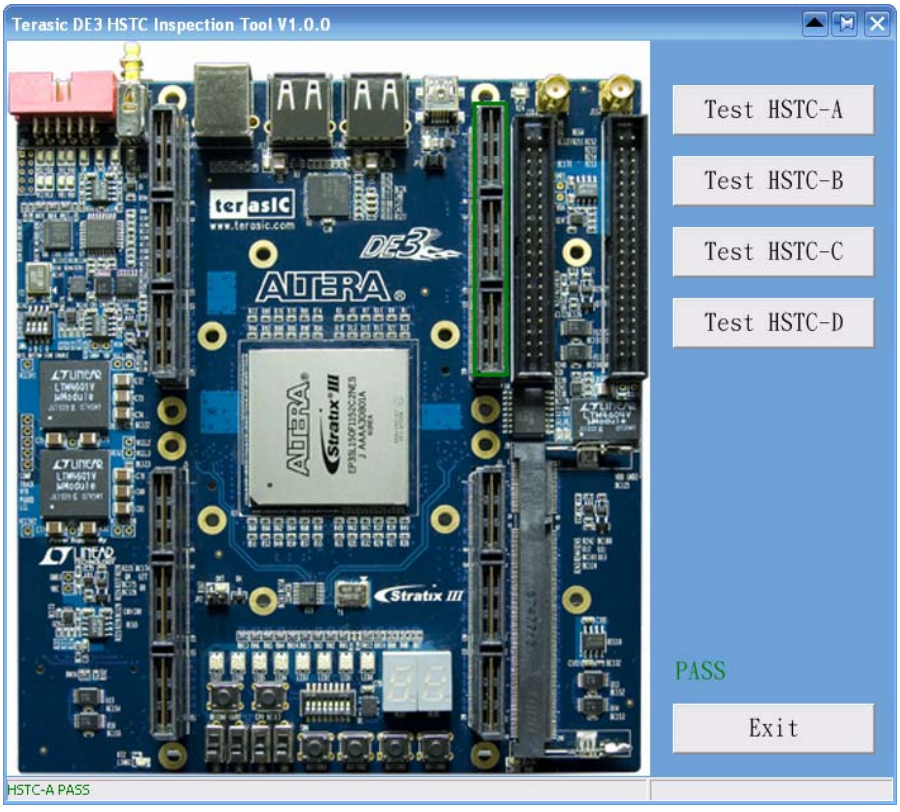


Figure D.4. The test result of the HSTC connector A

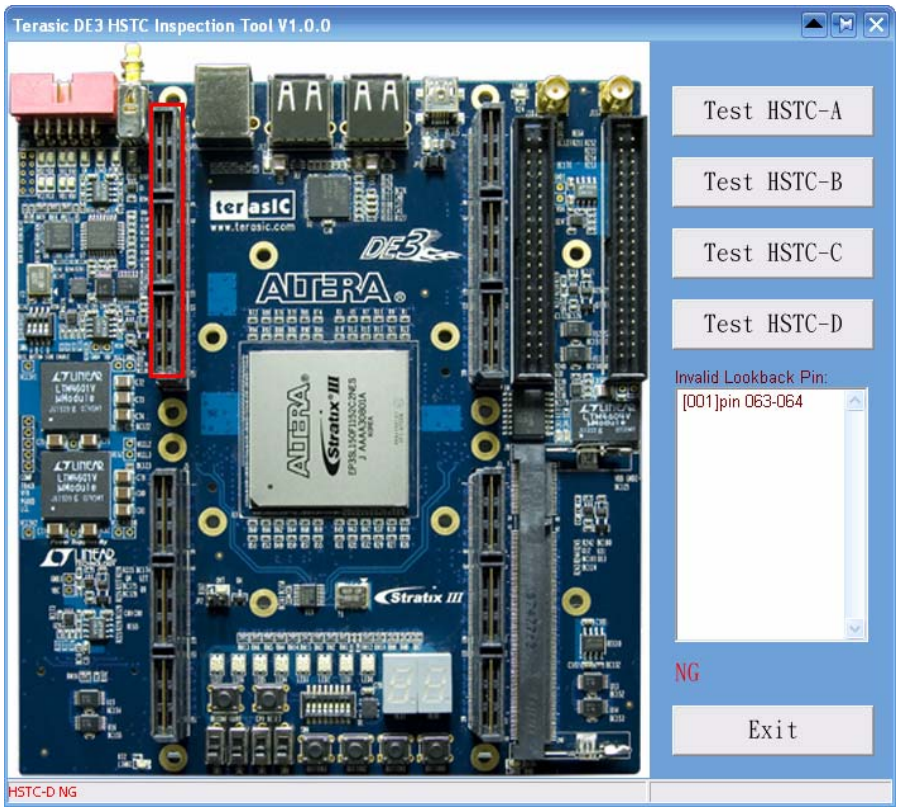


Figure D.5. The reported message of the invalid I/O pins

Appendix E

LVDS Termination Resistors

This chapter describes the distribution of LVDS termination resistors on DE3 board. The I/O pins of a HSTC connector on bank 2 and bank 3, which are used for differential transmitter channels, support emulated LVDS via a termination resistor, as illustrated in Figure E.1. The following tables list detailed distribution of termination resistors for each differential pin.

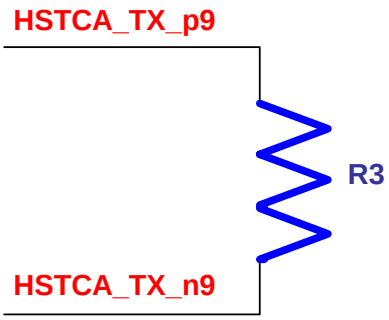


Figure E.1. The differential termination resistor on the differential transmitter channel

Table E-1 The distribution of the differential termination resistors for HSTC connector

Differential Pair	Signal Name	Part name of the differential termination resistor			
		HSTC A	HSTC B	HSTC C	HSTC D
9	TX_p9, TX_n9	R3	R27	R51	R75
10	TX_p10, TX_n10	R4	R28	R52	R76
11	TX_p11, TX_n11	R5	R29	R53	R77
12	TX_p12, TX_n12	R6	R30	R54	R78
13	TX_p13, TX_n13	R7	R31	R55	R79
14	TX_p14, TX_n14	R8	R32	R56	R80
15	TX_p15, TX_n15	R9	R33	R57	R81
16	TX_p16, TX_n16	R10	R34	R58	R82
17	TX_p17, TX_n17	R11	R35	R59	R83
18	TX_p18, TX_n18	R12	R36	R60	R84
19	TX_p19, TX_n19	R13	R37	R61	R85
20	TX_p20, TX_n20	R14	R38	R62	R86
21	TX_p21, TX_n21	R15	R39	R63	R87
22	TX_p22, TX_n22	R16	R40	R64	R88

Table E-2 The distribution of the differential termination resistors for HSTC connector					
Differential Pair	Signal Name	Part name of the differential termination resistor			
		HSTC A	HSTC B	HSTC C	HSTC D
23	TX_p23, TX_n23	R17	R41	R65	R89
24	TX_p24, TX_n24	R18	R42	R66	R90
25	TX_p25, TX_n25	R19	R43	R67	R91
26	TX_p26, TX_n26	R20	R44	R68	R92
27	TX_p27, TX_n27	R21	R45	R69	R93
28	TX_p28, TX_n28	R22	R46	R70	R94
29	TX_p29, TX_n29	R23	R47	R71	R95
CLK1_IN	HSTCA_CLKIN_n1, HSTCA_CLKIN_p1	R1	R25	R49	R73
CLK1_OUT	HSTCA_CLKOUT_n1, HSTCA_CLKOUT_p1	R2	R26	R50	R74

Additional Information

Getting Help

Here are the addresses where you can get help if you encounter problems:

- Altera Corporation
  101 Innovation Drive
  San Jose, California, 95134 USA
  Email: mysupport@altera.com

- Terasic Technologies
  No. 356, Sec. 1, Fusing E. Rd.
  Jhubei City, HsinChu County, Taiwan, 302
  Email: support@terasic.com
  Web: www.terasic.com

Revision History

Date	Version	Changes
2008.7	First publication	
2008.9	V1.1	• Modify Figure 2.12 • Add Appendix E
2008.11	V1.2	• Modify descriptions of POWER ON pin on HSTC connector. • Add section 5.4 DDR2 demonstration. • Modify section 2.2 • Add Figure 2.14 and Figure 2.15 • Modify Table A-12, Table A-12
2008.12.25	V1.2.1	• Modify Figure 2.14.
2009.1.5	V.1.2.2	• Modify Figure 2.12
2009.1.9	V.1.2.3	• Modify Figure 1.2 and Figure 1.4 • Modify section 1.2 and Appendix C