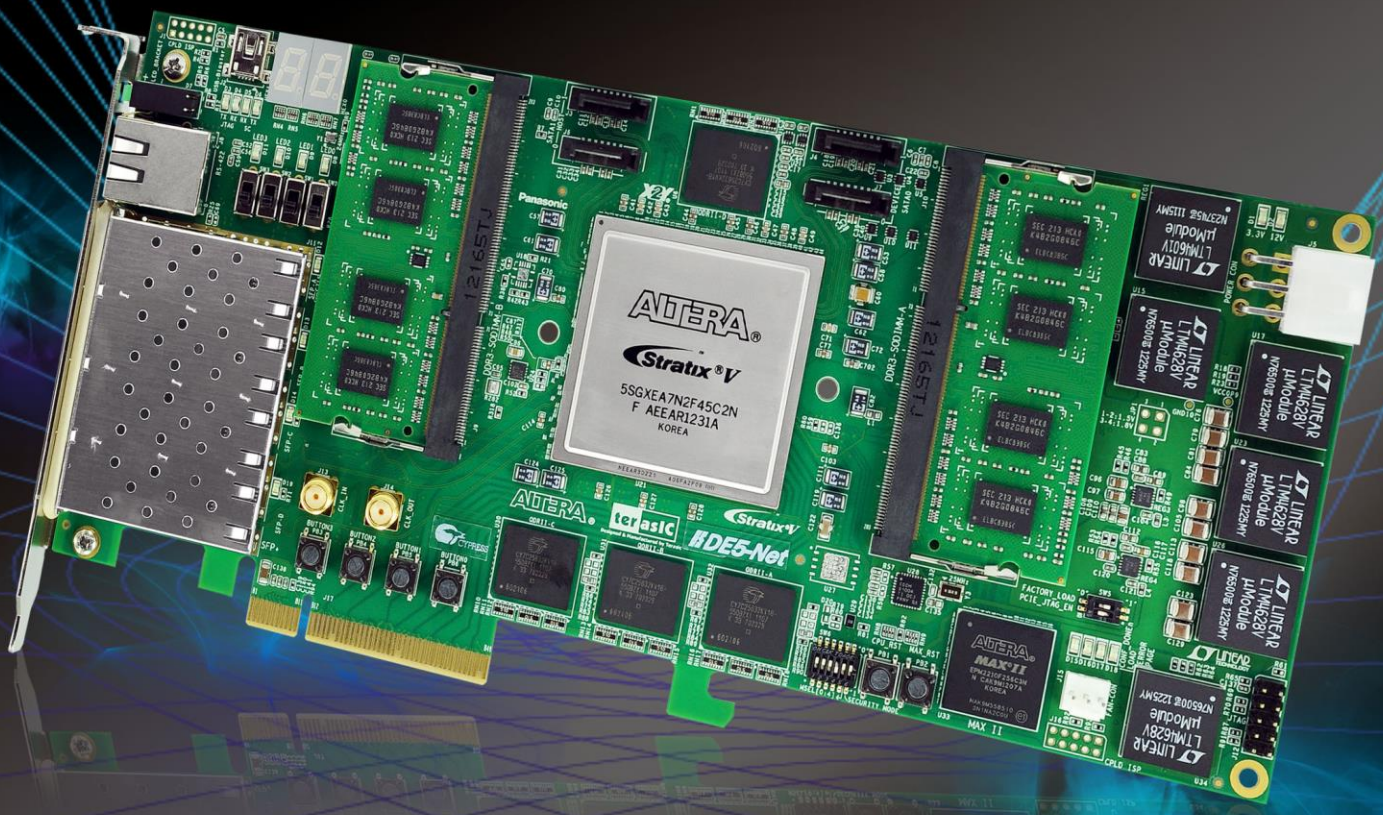
DE5-Net

OpenCL

OpenCL



Stratix V | Flash | PCI EXPRESS | DDR3 | QDRII+ | SFP+ | SERIAL ATA

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ALTERA

CONTENTS

Chapter 1

DE5-Net OpenCL

DE5-NET, an unparalleled and powerful platform for high-speed computation, is now officially also an Altera certified board for Altera's Preferred Board Partner Program for OpenCL. It supports both 64-bit Windows and Linux. This document will introduce you how to setup OpenCL development environment for DE5-NET board, and how to compile and execute the example projects for DE5-Net. Note that OpenCL coding instruction is not in the scope of this document, but the user can refer to Altera SDK for OpenCL Programming Guide for more details.

http://www.altera.com/literature/hb/opencl-sdk/aocl_programming_guide.pdf

1.1 System Requirement

The following items are required to set up OpenCL for DE5-NET board:

- Terasic DE5-NET Board with two 2GB DDR3-SODIMM installed
- A Host PC with
  - USB Host Port
  - One PCI Express x8/x16 slot with 12V power pin
  - 32GB memory is recommended, 24GB is minimal
  - 2x3 pin 12V Power for DE5-Net(optional)
- An USB Cable(type A to mini-B)
- 64-bit Windows7 or Linux Installed
- Altera Quartus II 13.1 Installed, licensed is required
- Altera OpenCL 13.1 Installed, license is required
- Visual Studio 2012 C/C++ installed for Windows7
- GNU development tools for Linux

Note, Altera OpenCL only supports 64-bit OS and x86 architecture.

1.2 OpenCL Architecture

An OpenCL project is composed of both OpenCL Kernel and Host Program as shown in **Figure 1-1**. OpenCL kernel is compiled with Altera OpenCL compiler provided by the Altera OpenCL SDK. The Host Program is compile by Visual Studio C/C++ in Windows or GCC on Linux.

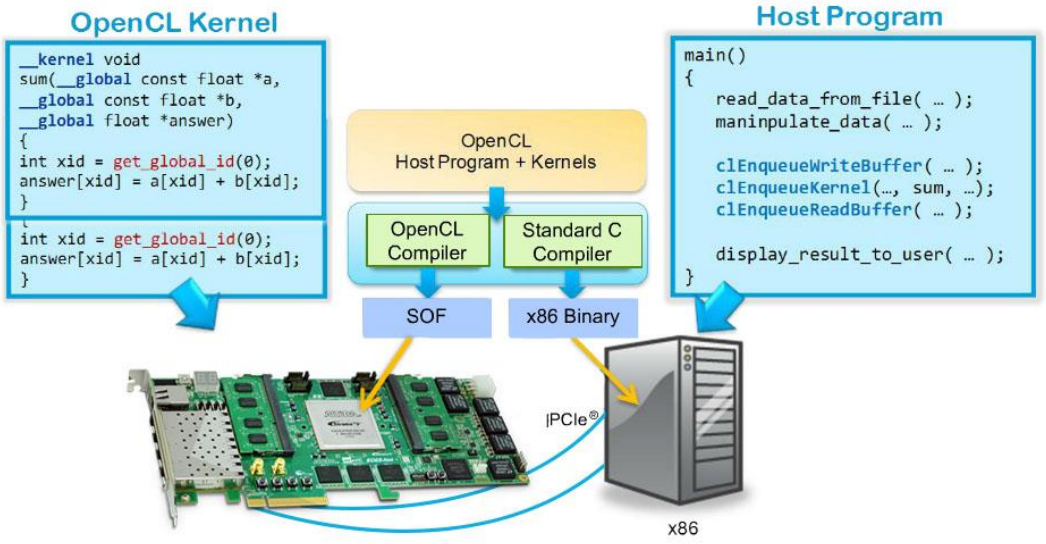

Figure 1-1 Altera OpenCL Architecture

Chapter 2

OpenCL for Windows

This chapter describes how to set up DE5-NET OpenCL development environment on 64-bit Windows, and how to compile and test the OpenCL examples for DE5-Net. For more details about Altera OpenCL started guide, please refer to:

http://www.altera.com/literature/hb/opencl-sdk/aocl_getting_started.pdf

2.1 Software Installation

This section describes where to get the required softwares for OpenCL.

■ Altera Quartus II and OpenCL SDK

Altera Quartus II and OpenCL SDK can be download from the web site:

http://dl.altera.com/opencl

For Quartus II installation, please make sure that the Stratix V device is included.

■ Visual Studio 2012

If developers don't have Visual studio C/C++ 2012, they can use the trial version of Visual Studio 2012 Express. The software can be downloaded from the web site:

http://www.microsoft.com/en-us/download/details.aspx?id=34673

■ DE5-NET OpenCL SDK

After Quartus II and OpenCL SDK are installed, copy the whole "terasic" folder in Terasic OpenCL Kit into the folder "C:\altera\13.1\hld\board" where assumed Quartus II is installed on the folder "C:\Altera \13.1". **Figure 2-1** shows file folder content when **terasic** folder is copied.

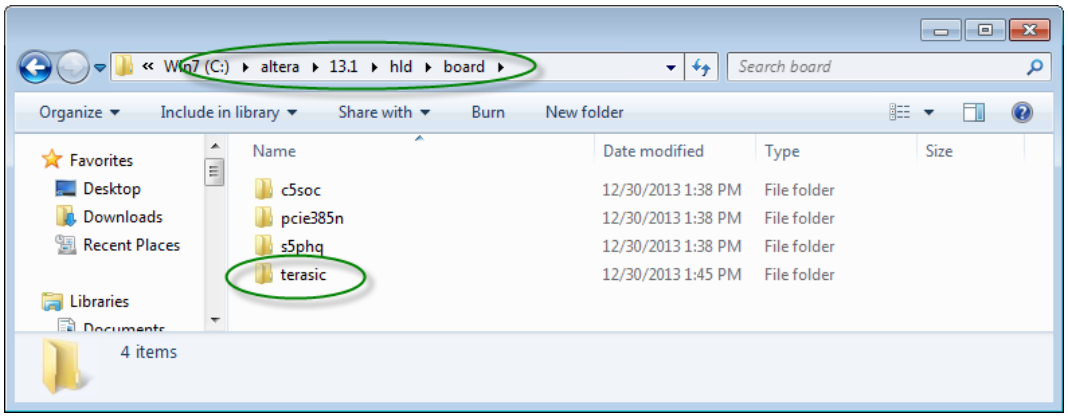

Figure 2-1 Copy Terasic Folder to hld/bolard Folder

2.2 OpenCL License Installation

An OpenCL license is required for Altera OpenCL SDK to compile any OpenCL projects successfully. Developers can purchase the OpenCL license from either Altera or Terasic. Assuming that developers have obtained a license file with the filename "license.dat", and it is saved in the local disk with the file path such as "c:\license.dat". The license can then be set up by creating an environment variable **LM_LICENSE_FILE**, and set its value as "c:\license.dat". Note that this environment value needs to correspond to the actual "license.dat" file location.

Now, here are the procedures to create the required **LM_LICENSE_FILE** environment variable on Windows 7:

1. Open the Start Menu and right click on **Computer**. Select **Properties**.
2. Select **Advanced system settings.**
3. In the **Advanced** tab, select **Environment Variables.**
4. Select **New**.
5. In the popup **New User Variable** dialog as shown in **Figure 2-2**, type "**LM_LICENSE_FILE**" in the **Variable name** edit box and type "**c:\license.dat**" in the **Variable value** edit box.

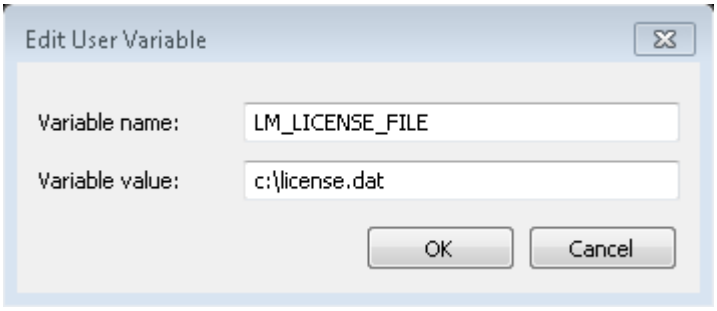

Figure 2-2 Setup LM_LICENSE_FILE Environment Variable

2.3 Configure

For Altera OpenCL SDK to be able to find the kit location of DE5-NET correctly, developers need to create an environment variable **AOCL_BOARD_PACKAGE_ROOT**, and set its value as:

"%ALTERAOCLSDKROOT%\board\terasic\de5net"

Here are the procedures to create the required **AOCL_BOARD_PACKAGE_ROOT** environment variable on Windows 7:

1. Open the Start Menu and right click on **Computer**. Select **Properties**.
2. Select **Advanced system settings.**
3. In the **Advanced** tab, select **Environment Variables.**
4. Select **New**.
5. In the popup **New User Variable** dialog as shown in **Figure 2-3**, type "**AOCL_BOARD_PACKAGE_ROOT**" in the **Variable name** edit box and type "**%ALTERAOCLSDKROOT%\board\terasic\de5net**" in the **Variable value** edit box.
6. In Command Prompt window, type "aocl install" to install PCI Express driver. Note that users need to have administrator privileges to install the driver.

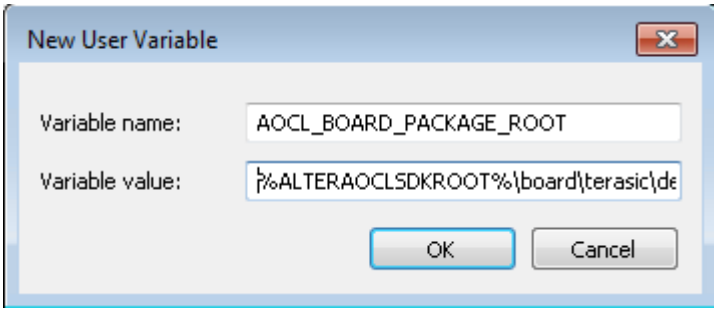

Figure 2-3 Setup AOCL_BOARD_PACKAGE_ROOT Environment Variable

2.4 Board Setup

Before testing OpenCL on DE5-NET, please following below procedures to set up DE5-NET board on your PC as shown in **Figure 2-4**.

1. Make sure your PC is powered off.
2. Insert DE5-NET board into PCI Express x8 or x16 slot.
3. Connect PC's 12V PCI Express 6-pin power source to the DE5-NET
4. Connect PC's USB port to DE5-NET mini USB port using an USB cable.

Note, the usb cable can be removed later if OpenCL code had been programming to the startup configuration flash of DE5-NET by 'aocl flash' command.

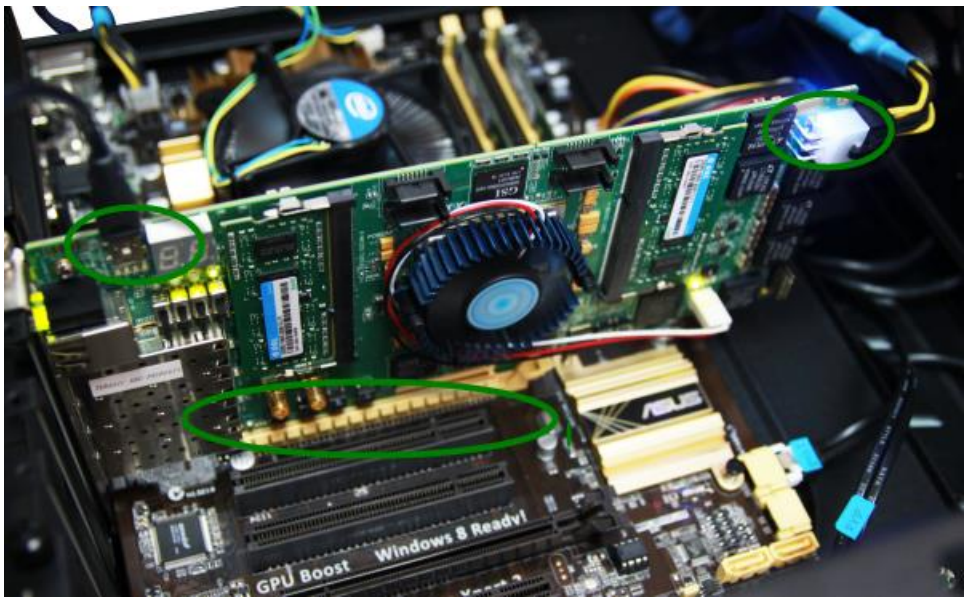

Figure 2-4 Setup DE5-NET board on PC

2.5 OpenCL Environment Verify and Flash CvP

This section will show how to make sure the OpenCL environment is setup correctly. First, please open **Command Prompt** windows by click Windows **Start** button, clicking **All Programs**, clicking **Accessories**, and then click **Command Prompt**.

■ Target Board

In Command Prompt window, type “aoc --list-boards” command, and make sure “de5net_a7” is listed in **Board list** as shown in **Figure 2-5**.

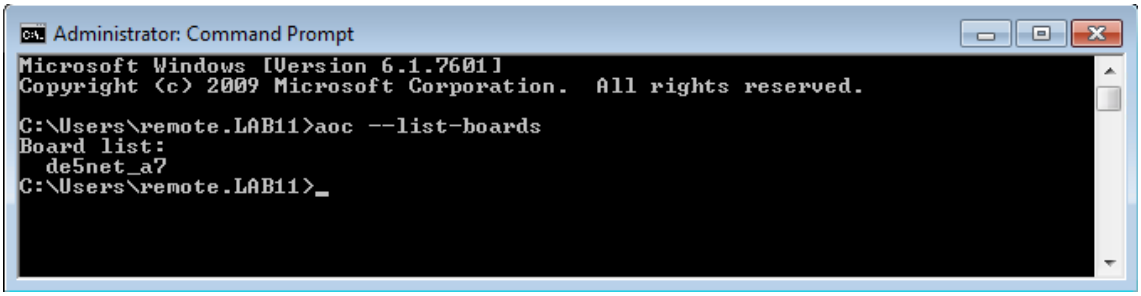

Figure 2-5 ‘de5net_a7’ is listed in Board list

■ Test ‘aocl program’ Command

In Command Prompt window, type “cd C:\altera\13.1\hld\board\terasic\tests\blank” to go to **blank** OpenCL project folder, then type “aocl program blank.aocx” to configure the FPGA of DE5-NET with **blank.aocx** OpenCL image. First, the programmer will try to configure the FPGA of DE5-NET through PCI Express CvP(Configuration via Protocol). If the CvP is not found, the programmer will extract reprogram_temp.sof from the blank.aocx and try to use reprogram_temp.sof to configure the FPGA through USB-Blaster as shown in **Figure 2-6**. It is normal for the programmer not being able to find CvP for the first time, because the startup configuration on flash of DE5-NET does not contain required CvP. Next section will show how to use “aocl flash” command to write a CvP enabled startup configuration on flash.

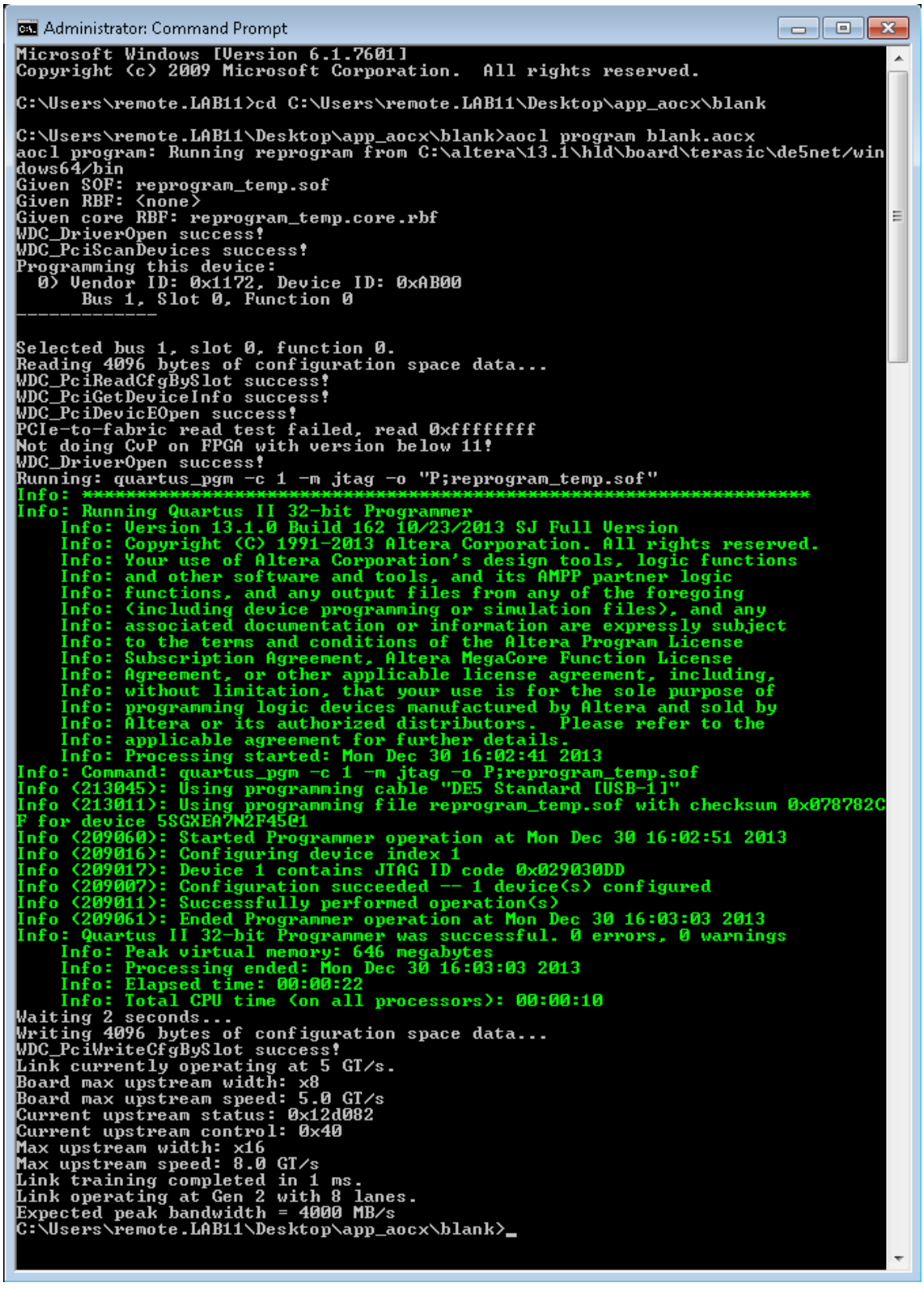

Figure 2-6 'aocl program blank.aocx' Command

■ Test 'aocl flash' Command

In Command Prompt window, type "cd C:\altera\13.1\hld\board\terasic\tests\blank" to go to blank OpenCL project folder, then type "aocl flash blank.aocx" to write **blank.aocx** OpenCL image onto the startup configuration flash of DE5-NET. Before flash programming, the programmer will ask users which startup configuration image area will be used as shown in **Figure 2-7**. This is because DE5-NET provides two startup configuration image areas, called as Factory Image and User Image. We recommend users to keyin '1' to select User Image area.

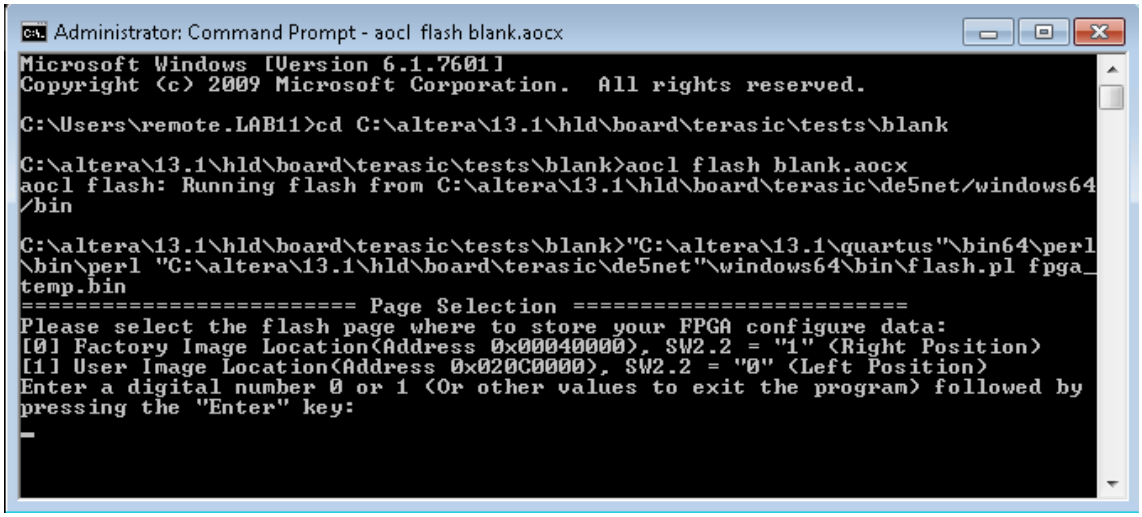

Figure 2-7 Select Flash Page

After users select desired flash area, it will take about 20 minutes for flash programming. **Figure 2-8** is the screen shot when flash programming is done successfully.

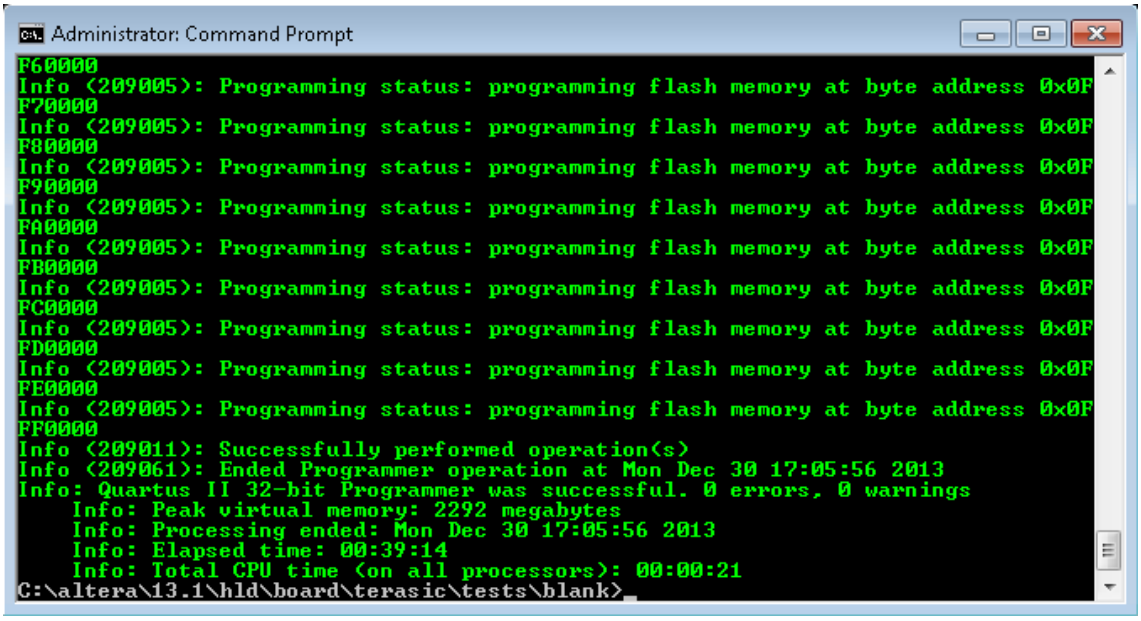

Figure 2-8 'aocl flash blank.aocx" successfully

To make sure a correct image is used when FPGA boots up, please make sure the dip switch SW2.2 on DE5-NET is changed to the correct location. If a User Image area is selected, the dip switch SW2.2 on the DE5-NET should be moved to **left** position as shown in **Figure 2-9.**

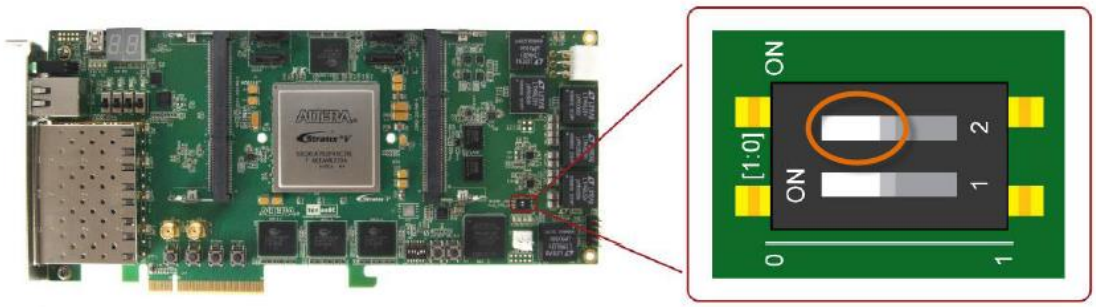

Figure 2-9 Set SW2.2 to Left Position (User Image Page)

After flash programming is done successfully and SW2.2 is set to correct position, developers can power off PC and turn it back on and check whether the **blank** OpenCL image, which is CvP enabled, configures the FPGA successfully. In Command Prompt window, type "cd C:\altera\13.1\hld\board\terasic\tests\blank" to go to blank project folder, then type "aocl program blank.aocx" to configure the FPGA with **blank.aocx** OpenCL image. If the programing message displays "CvP worked" as shown in **Figure 2-10**, it means the **blank** OpenCL image is programmed into the flash correctly and CvP works well.

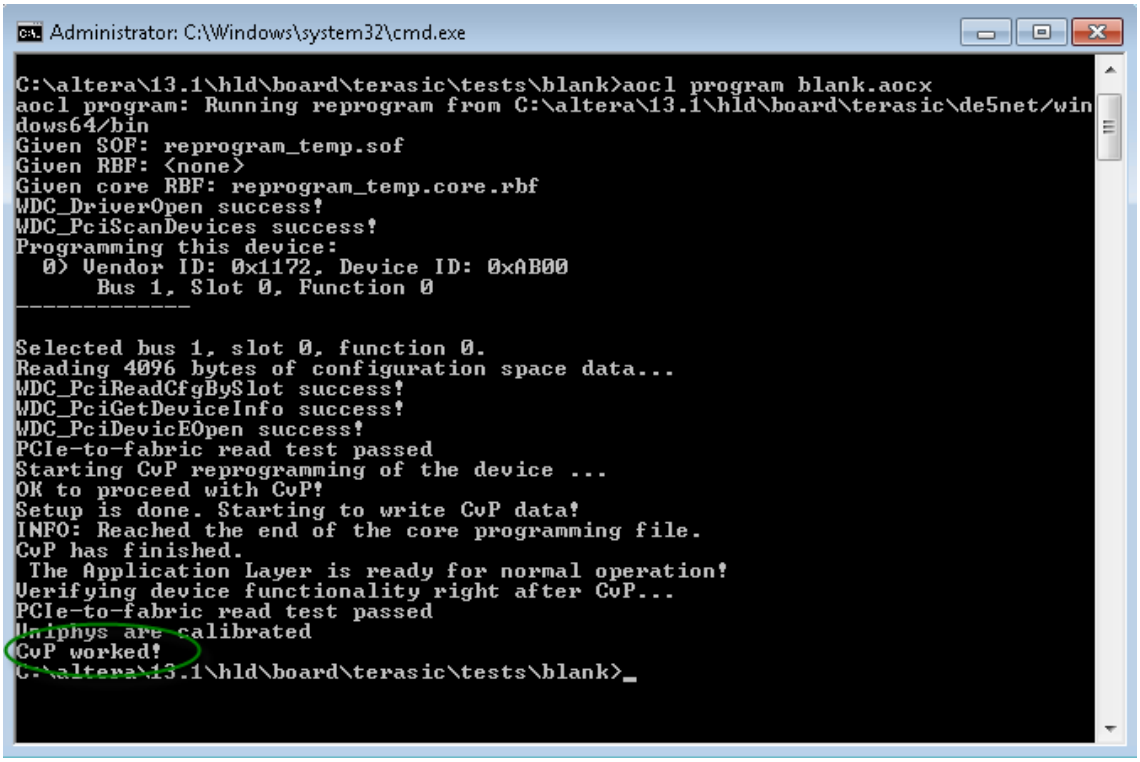

Figure 2-10 'aocl program blank.aocx" use CvP

2.6 Compile and Test OpenCL Project

This section will show how to compile and test OpenCL kernel and OpenCL Host Program for the boardtest project. Developers can use the same procedures to compile and test other OpenCL examples for DE5-NET.

■ Compile OpenCL Kernel

The utility **aoc** (Altera SDK for OpenCL Kernel Compiler) is used to compile OpenCL kernel. In Command Prompt window, type "cd C:\altera\13.1\hld\board\terasic\tests\boardtest" to go to **boardtest** project folder, then type "aoc boardtest.cl --sw-dimm-partition" to compile the OpenCL kernel. It will take about one hour for compiling. When the compilation process is finished, OpenCL image file boardtest.aocx is generated. **Figure 2-11** is the screenshot when OpenCL kernel is compiled successfully. For required parameters to compile boardtest.cl, please refer to the README.txt that is in the same folder as the boardtest.cl. For detailed usage of **aoc**, please refer to the **Altera SDK for OpenCL Programming Guide**:

http://www.altera.com/literature/hb/opencl-sdk/aocl_programming_guide.pdf

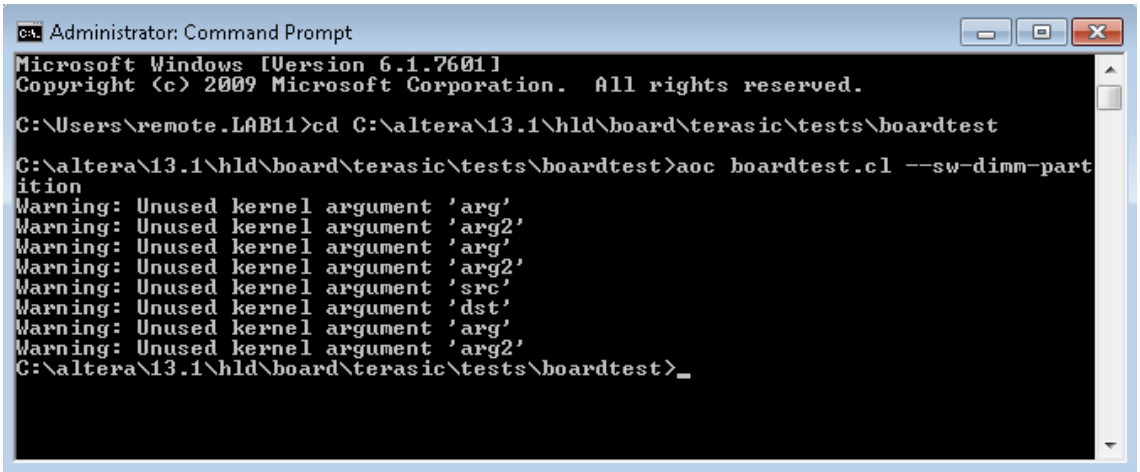

Figure 2-11 'aoc boardtest.cl" OpenCL kernel compile successfully

■ Compile Host Program

Visual Studio C/C++ 2012 is used to compile the Host Program. Launch Visual Studio, and select menu item "FILE→Open Project…". In the Open Project dialog, go to the folder "C:\altera\13.1\hld\board\terasic\tests\boardtest\host", and select "boardtest.sln" as shown **Figure 2-12**.

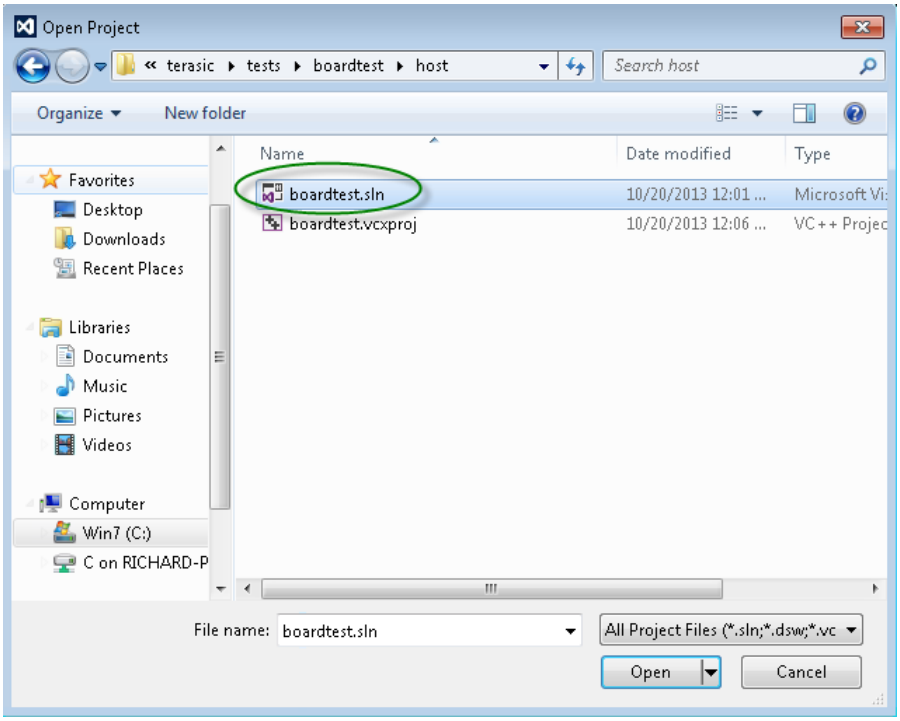

Figure 2-12 Open bloardtest.sln Host Program

After boardtest Host Program project is opened successfully, in Visual Studio IDE select menu item "BUILD→Build Solution" to build host program. When build is successfully, you will see successful message as show in **Figure 2-13**. The execute file is generate in:

"C:\altera\13.1\hld\board\terasic\tests\boardtest\host\x64\Release\boardtest.exe"

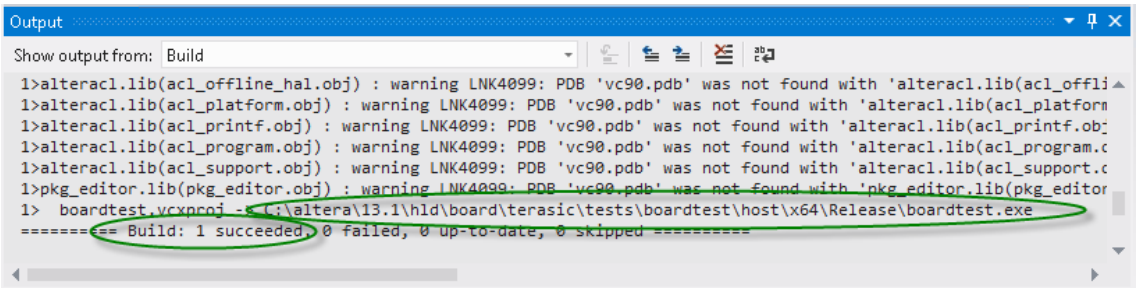

Figure 2-13 Message for boardtest Host Program build successfully

■ Test boardtest project

First, use the compiled OpenCL image file boardtest.aocx to configure the FPGA. In Command Prompt window, type "cd C:\altera\13.1\hld\board\terasic\tests\boardtest" to go to **boardtest** project folder, then type "aocl program boardtest.aocx" to configure FPGA with the OpenCL Image boardtest.aocx. If configuration is successfully, you will see the successful message as shown in **Figure 2-14.**

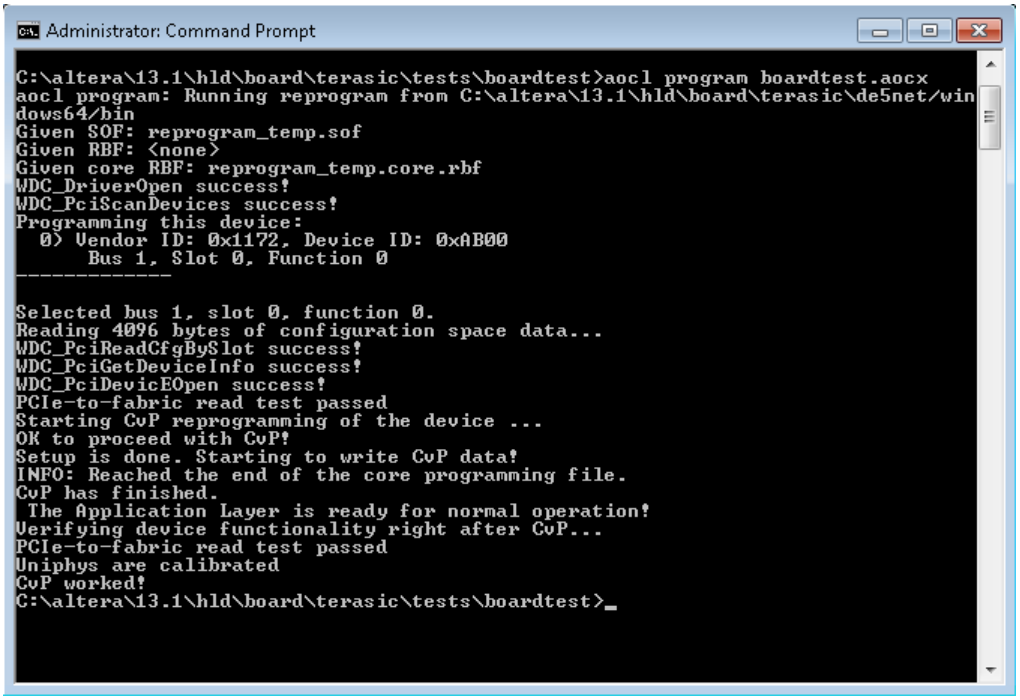

Figure 2-14 "aocl program boardtest.aocx" configured successfully

Then, launch the compiled Host Program to start boardtest executable file for testing. Please copy "C:\altera\13.1\hld\board\terasic\tests\boardtest\host\x64\Release\boardtest.exe" to the folder "C:\altera\13.1\hld\board\terasic\tests\boardtest". In Command Prompt window, type "cd C:\altera\13.1\hld\board\terasic\tests\boardtest" and execute "boardtest.exe". **Figure 2-15** is the screen shot when the test is successful.

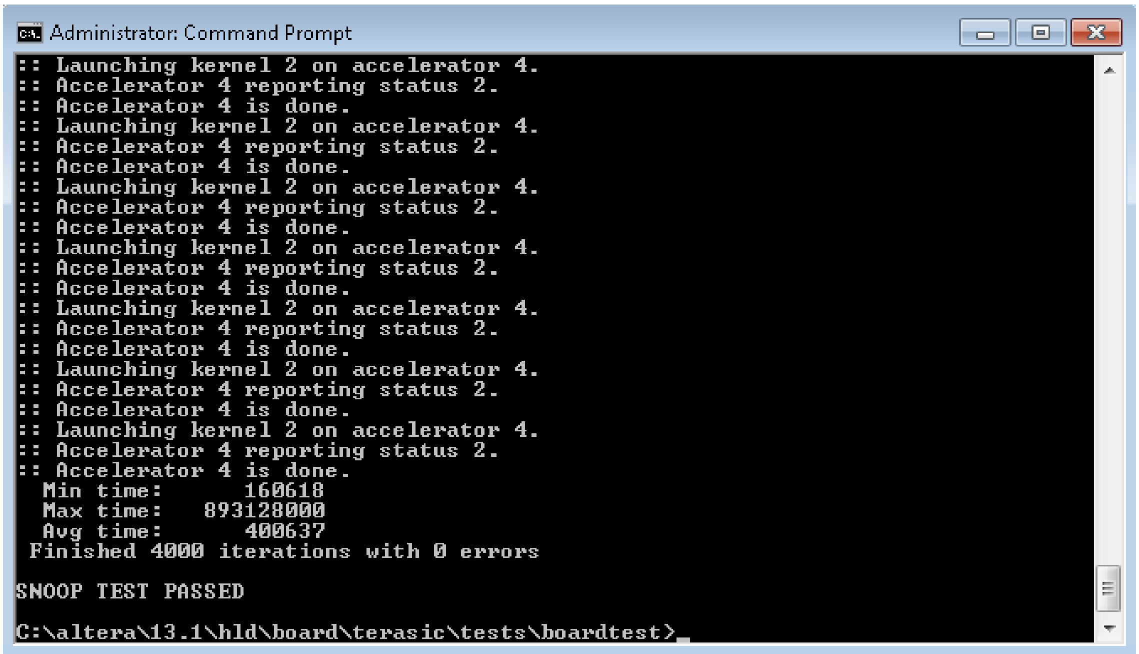

Figure 2-15 "boardtest" test successfully

Chapter 3

OpenCL for Linux

This chapter describe how to setup DE5-NET OpenCL development environment on 64-bit Linux (Red Hat Enterprise Linux 5.6 or later and CentOS 6.4 or later are recommended), and how to compile and test the OpenCL examples for DE5-Net. For more details about Altera OpenCL , please refer to Altera SDK for OpenCL Getting Started document:

http://www.altera.com/literature/hb/opencl-sdk/aocl_getting_started.pdf

3.1 Software Installation

This section describes how to download and install the required software for OpenCL.

■ Altera Quartus II and OpenCL

Altera Quartus II and OpenCL can be download from the web site:

http://dl.altera.com/opencl/

open the link and select the Linux operation system and the needed version(default the latest) as **Figure 3-1** shows.

Figure 3-1 OpenCL Linux version selection

In the OpenCL software download selection form, choose and click the Altera FPGA Design Software and SDK for OpenCL as **Figure 3-2** show. if selected Altera FPGA Design software, please make sure the Stratix V device is included.

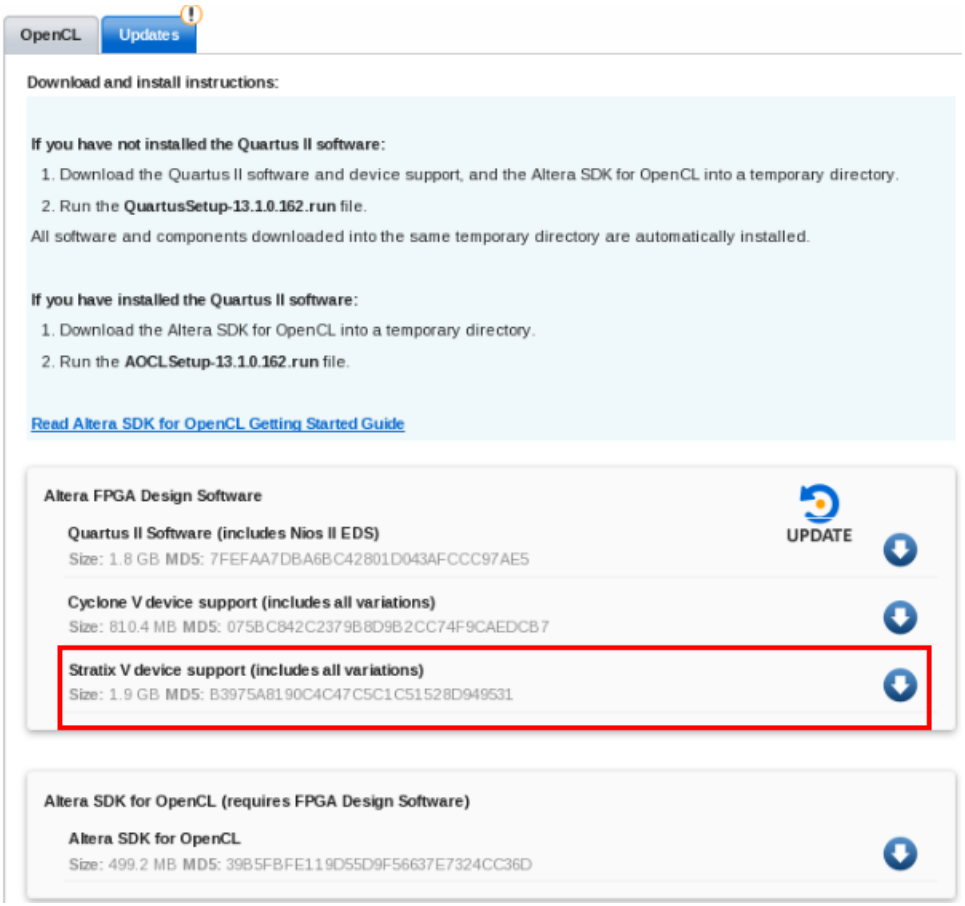

Figure 3-2 OpenCL Linux version download

Quartus II software uses the built-in USB-Blaster II drivers on Linux to access USB-Blaster II

download cable on DE5-Net. but after installed the Quartus II software with built-in drivers, User need to change the port permission for USB-Blaster II via issuing

'gedit /etc/udev/rules.d/51-usbblaster.rules'

to create and add the following lines to the **/etc/udev/rules.d/51-usbblaster.rules** file.

```
# USB-Blaster
BUS=="usb", SYSFS{idVendor}=="09fb", SYSFS{idProduct}=="6001", MODE="0666"
BUS=="usb", SYSFS{idVendor}=="09fb", SYSFS{idProduct}=="6002", MODE="0666"
BUS=="usb", SYSFS{idVendor}=="09fb", SYSFS{idProduct}=="6003", MODE="0666"
# USB-Blaster II
BUS=="usb", SYSFS{idVendor}=="09fb", SYSFS{idProduct}=="6010", MODE="0666"
BUS=="usb", SYSFS{idVendor}=="09fb", SYSFS{idProduct}=="6810", MODE="0666"
```

Note: You must have system administration (root) privileges to configure the USB-Blaster download cable drivers.

■ GNU development tools

GNU development tools such as **gcc**(include **g++**) and **make** are required to build the driver and application under Linux. User can issue 'yum install gcc ccompat-gcc-34-c++ make' command to download and install them and their dependencies via internet.

Note: To install the SDK on Linux, you must install it in a directory that you own (that is, a directory that is not a system directory). You must also have sudo or root privileges.

■ DE5-NET openCL BSP

After Quartus II and OpenCL SDK are installed, copy the whole "terasic" folder in Terasic OpenCL Kit into the folder "/root/altera/13.1/hld/board" where assumed Quartus II is installed on the folder "/root/altera/13.1". **Figure 3-3** shows file folder content when **terasic** folder is copied.

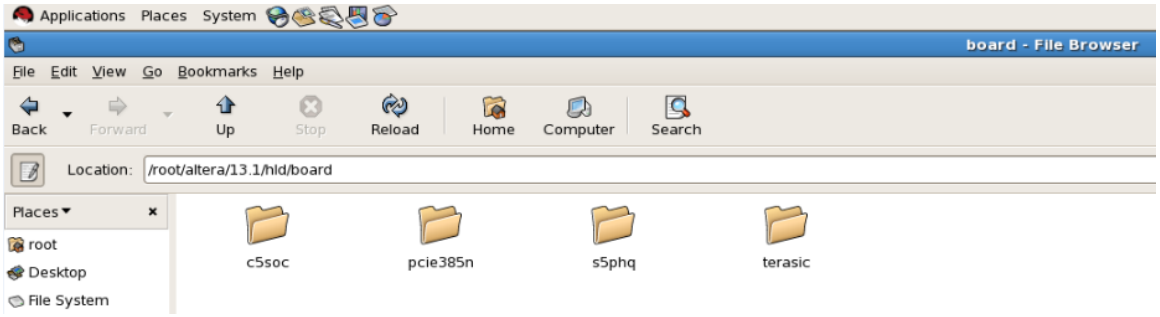

Figure 3-3 Copy Terasic Folder to hld/bolard Folder

3.2 OpenCL License Installation

An OpenCL license is required to compile the OpenCL projects for Altera OpenCL SDK. Developers can purchase the OpenCL license from either Altera or Terasic. Assuming that developers have obtained a license file with the filename "license.dat", and it is saved in the local disk with the file path such as "/root/altera/13.1/hld/license.dat". The license can then be set up by creating an environment variable **LM_LICENSE_FILE**, and set its value as "/root/altera/13.1/hld/license.dat".

Note that this environment value needs to correspond to the actual "license.dat" file location.

The next chapter will describe the license environment setting up.

3.3 Configure

If you install the ALTERA FPGA development software and OpenCL SDK on a system that does not contain any .cshrc or Bash Resource file (.bashrc) in your directory, you must set the ALTERAOCLSDKROOT and PATH environment variables manually. And for Altera OpenCL SDK able to find the kit location of DE5-NET correctly, the developers need to create an environment variable for the DE5-NET board **AOCL_BOARD_PACKAGE_ROOT**, and set its value as:

"%ALTERAOCLSDKROOT%\board\terasic\de5net"

Alternatively, you can edit the "/etc/profile" **profile** file, and append the environment variables to it.

To do this type "*gedit /etc/profile" command on Linux Terminal* to open the **profile** file by the **gedit** editor tool, and append the following setting to the **profile** file. Then, save the file and type "*source /etc/profile"* command in Linux Terminal to make the settings make effect.

```
export QUARTUS_ROOTDIR=/root/altera/13.1/quartus
export ALTERAOCLSDKROOT=/root/altera/13.1/hld
export PATH=$PATH:"$QUARTUS_ROOTDIR"/bin: "$ALTERAOCLSDKROOT"/linux64/bin
export LD_LIBRARY_PATH="$ALTERAOCLSDKROOT"/linux64/lib
export AOCL_BOARD_PACKAGE_ROOT="$ALTERAOCLSDKROOT"/ board/terasic/de5net
export QUARTUS_64BIT=1
export LM_LICENSE_FILE= /root/altera/13.1/hld/license.dat
```

3.4 Board Setup

Before testing OpenCL on DE5-NET, please following the below procedure to setup DE5-NET board on your PC as shown in **Figure 3-4**.

1. Make sure your PC is power off.
2. Insert DE5-NET board into PCI Express x8 or x16 slot.
3. Connect PC's 12V PCI Express 6-pin power to the DE5-NET source (if there's not, ignore this step)
4. Connector PC's USB port to DE5-NET mini USB port using an USB cable.

Note, the usb cable can be removed later if any one of OpenCL code had been programming to the startup configuration flash of DE5-NET by 'aocl flash' command.

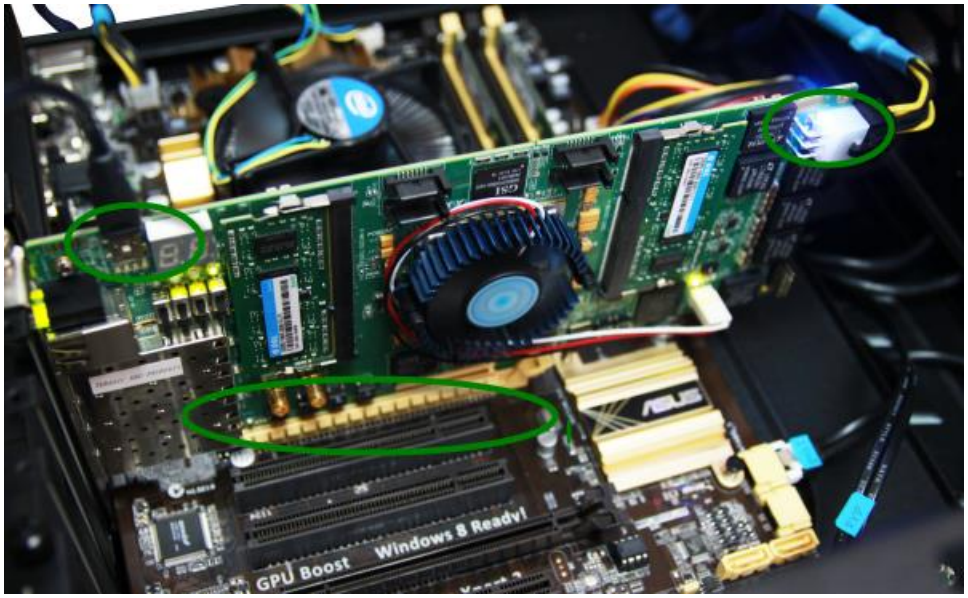

Figure 3-4 Setup DE5-NET board on PC

3.5 OpenCL Environment Verify and Flash CvP

This section will show how to make sure the OpenCL environment is setup correctly.

Firstly, please open the Linux system **terminal** window by right click the Mouse on system desktop, then clicking on **Open Terminal**.

■ Target Board

In the Linux terminal, type "*aoc --list-boards"* command, and make sure "de5net_a7" is listed in **Board list** as shown in **Figure 3-5**.

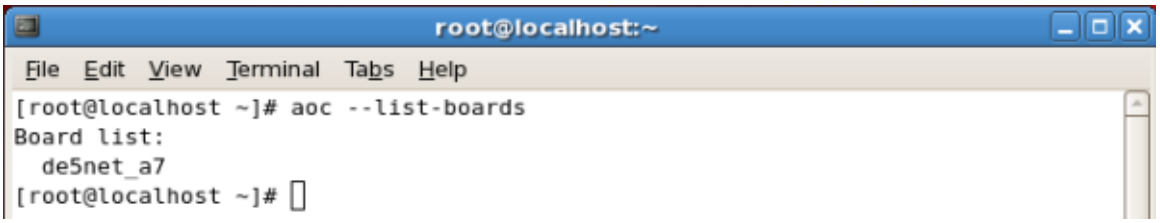

Figure 3-5 'de5net_a7' is listed in Board list

Then type "*aocl install"* to load the PCIe driver for the DE5-NET as shown in **Figure 3-6**.

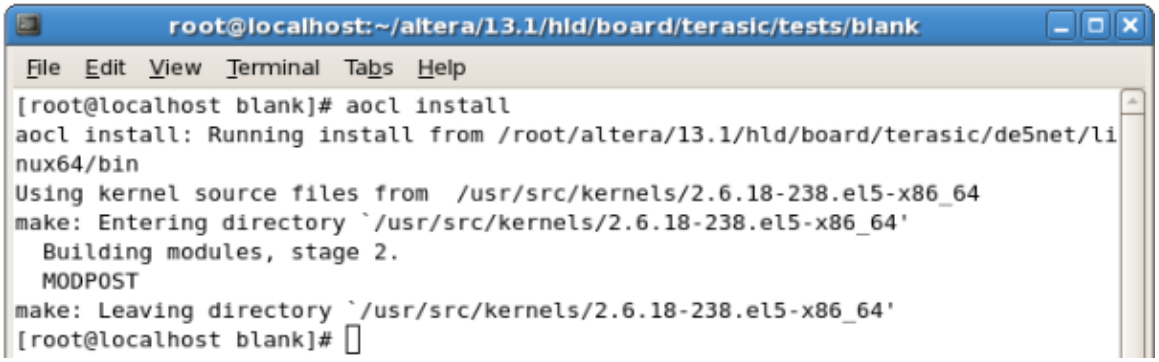

Figure 3-6 driver installation

Note: if user don't using the recommended Linux system or different version, recompile the driver is needed. You can compile it by typing

"cd root/altera/13.1/hld/board/terasic/de5net/host/linux64/driver" (there are source code, makefile and readme.txt)to *locate at the* driver source code directory and type *"./make_all"* to compile and generate the new driver. Before that, user need to install the kernel related development package matched the current kernel (**kernel-devel** package) via issuing '*yum install kernel-devel*' command.

■ Test 'aocl program' Command

In the Linux terminal, type "*cd /root/altera/13.1/hld/board/terasic/tests/blank"* to go to **blank** OpenCL project folder, then type "*aocl program blank.aocx"* to configure the FPGA of DE5-NET with **blank.aocx** OpenCL image.

Firstly, the programmer will try to configure the FPGA of DE5-NET through PCI Express CvP(Configuration via Protocol). If the CvP is not found, the programmer will extract reprogram_temp.sof from the blank.aocx and try to use reprogram_temp.sof to configure the FPGA through USB-Blaster as shown in **Figure 3-7**. It is normal for the programmer can't find CvP at first time, because the startup configuration on flash of DE5-NET does not contain required CvP Periphery image file.

Next section will show how to use "aocl flash" command to write a CvP enabled startup configuration on flash.

```
[root@localhost blank]# aocl program blank.aocx
aocl program: Running reprogram from /root/altera/13.1/hld/board/terasic/de5net/
linux64/bin
Device   : acl0
Given SOF: reprogram_temp.sof
Given RBF: (null)
Given core RBF: reprogram_temp.core.rbf
Saving PCI control registers of the board.
PCIe-to-fabric read test failed, read 0xffffffff
Not doing CvP since test_read failed!
Need to program the board via SOF
Programming the board with new SOF.
Executing: quartus_pgm -c 1 -m jtag -o "P;reprogram_temp.sof"
Info: *******************************************************************
Info: Running Quartus II 64-Bit Programmer
    Info: Version 13.1.0 Build 162 10/23/2013 SJ Full Version
    Info: Copyright (C) 1991-2013 Altera Corporation. All rights reserved.
    Info: Your use of Altera Corporation's design tools, logic functions
    Info: and other software and tools, and its AMPP partner logic
    Info: functions, and any output files from any of the foregoing
    Info: (including device programming or simulation files), and any
    Info: associated documentation or information are expressly subject
    Info: to the terms and conditions of the Altera Program License
    Info: Subscription Agreement, Altera MegaCore Function License
    Info: Agreement, or other applicable license agreement, including,
    Info: without limitation, that your use is for the sole purpose of
    Info: programming logic devices manufactured by Altera and sold by
    Info: Altera or its authorized distributors.  Please refer to the
    Info: applicable agreement for further details.
    Info: Processing started: Mon Feb 17 21:38:31 2014
Info: Command: quartus_pgm -c 1 -m jtag -o P;reprogram_temp.sof
Info (213045): Using programming cable "DE5 Standard [USB 1-1.3]"
Info (213011): Using programming file reprogram_temp.sof with checksum 0x07875E5
F for device 5SGXEA7N2F45@1
Info (209060): Started Programmer operation at Mon Feb 17 21:38:47 2014
Info (209016): Configuring device index 1
Info (209017): Device 1 contains JTAG ID code 0x029030DD
Info (209007): Configuration succeeded -- 1 device(s) configured
Info (209011): Successfully performed operation(s)
Info (209061): Ended Programmer operation at Mon Feb 17 21:38:58 2014
Info: Quartus II 64-Bit Programmer was successful. 0 errors, 0 warnings
    Info: Peak virtual memory: 964 megabytes
    Info: Processing ended: Mon Feb 17 21:38:58 2014
    Info: Elapsed time: 00:00:27
    Info: Total CPU time (on all processors): 00:00:08
Restoring PCI control registers of the board.
Link is operating as PCIe gen2 x 8
Vendor id = 0x1172, device id = 0xab00
[root@localhost blank]#
```

Figure 3-7 'aocl program blank.aocx' Command

■ Test 'aocl flash' Command

In the terminal, type "*cd /root/altera/13.1/hld/board/terasic/tests/blank"* to go to blank OpenCL project folder, then type "*aocl flash blank.aocx"* to program **blank.aocx** OpenCL image onto the

startup configuration flash of DE5-NET.

Before flash programming, the programmer will ask users which startup configuration image area will be used as shown in **Figure 3-8**. This is because DE5-NET provides two startup configuration image areas, called as Factory Image and User Image. Typing '1' to select User Image area is recommended.

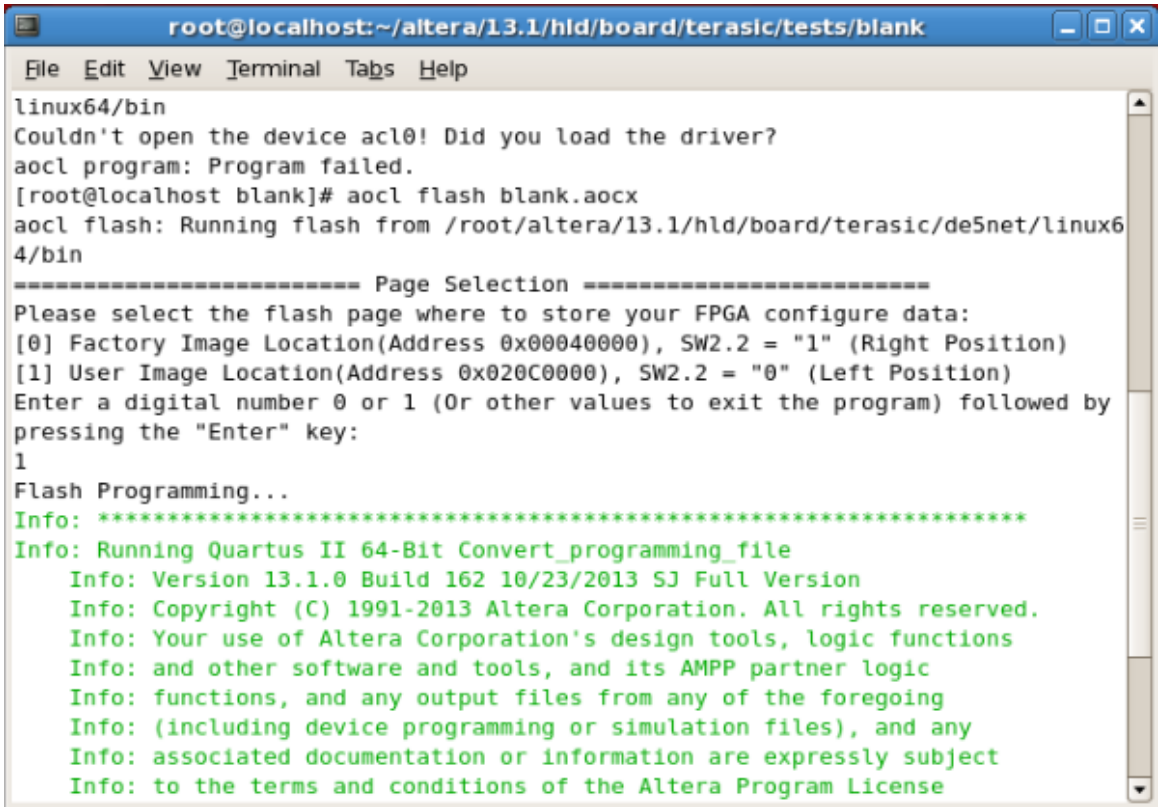

Figure 3-8 Select Flash Page

After selecting the desired flash area, it will take about 20 minutes for flash programming. **Figure 3-9** is the screen shot when flash programming is done successfully.

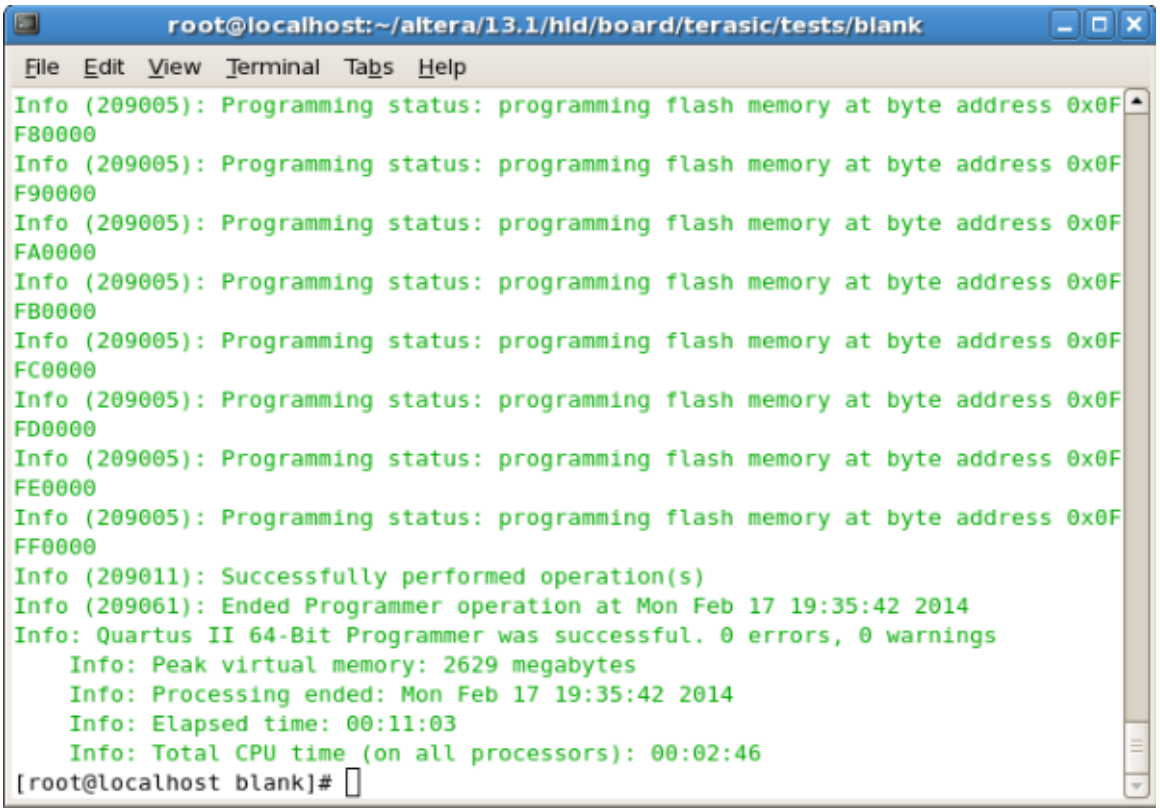

Figure 3-9 'aocl flash blank.aocx" successfully

To make sure correct image is used when FPGA boot, please make sure the dip switch SW2.2 on DE5-NTE is located at correct location. If User Image area is selected, the dip switch SW2.2 on the DE5-NET should be move to **left** position as shown in **Figure 3-10**.

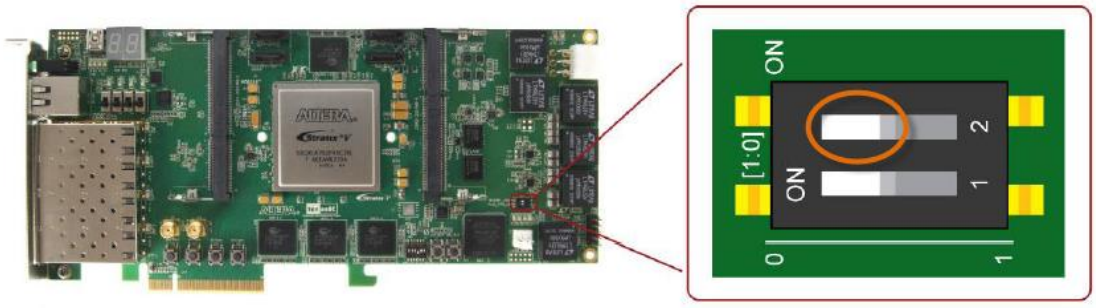

Figure 3-10 Set SW2.2 to Left Position (User Image Page)

After flash programming is done successfully and SW2.2 is set to correct position, developers can reboot the PC and check whether the **blank** OpenCL image, which is CvP enabled, configures the FPGA successfully when DE5-NET is power on. In the Linux terminal, type "*cd /root/altera/13.1/hld/board/terasic/tests/blank"* to go to blank project folder, then type "*aocl program blank.aocx"* to configure the FPGA with **blank.aocx** OpenCL image. If the programing

message displays "CvP worked" as shown in **Figure 3-11**, it means the **blank** OpenCL image is programmed into the flash correctly and CvP works well.

```
[root@localhost blank]# aocl program blank.aocx
aocl program: Running reprogram from /root/altera/13.1/hld/board/terasic/de5net/
linux64/bin
Device   : acl0
Given SOF: reprogram_temp.sof
Given RBF: (null)
Given core RBF: reprogram_temp.core.rbf
Saving PCI control registers of the board.
PCIe-to-fabric read test passed
Starting CvP reprogramming of the device with 33677312 bytes of data ...
PCIe-to-fabric read test passed
Uniphys are calibrated
CvP worked!
Restoring PCI control registers of the board.
Link is operating as PCIe gen2 x 8
Vendor id = 0x1172, device id = 0xab00
[root@localhost blank]#
```

Figure 3-11 'aocl program blank.aocx" use CvP

3.6 Compile and Test OpenCL Project

This section will show how to compile and run the OpenCL kernel and OpenCL Host Program for the boardtest example project. Developers can use the same procedures to compile and test other OpenCL examples (included in the kit) for DE5-NET.

■ Compile OpenCL Kernel

In the terminal, type "*cd /root/altera/13.1/hld/board/terasic/tests/boardtest"* to go to **boardtest** project folder, then type "*aoc boardtest.cl --sw-dimm-partition --report"* to compile the OpenCL kernel. It will takes about one hour for compiling. After that, the OpenCL image file boardtest.aocx is generated. **Figure 3-12** is the screen shot when OpenCL kernel is compiled successfully. For required parameters to compile boardtest.cl, please refer to the README.txt that is in the same directory.

The utility **aoc** (Altera SDK for OpenCL Kernel Compiler) is used to compile OpenCL kernel. For detailed usage of **aoc**, please refer to the **Altera SDK for OpenCL Programming Guide**:

http://www.altera.com/literature/hb/opencl-sdk/aocl_programming_guide.pdf

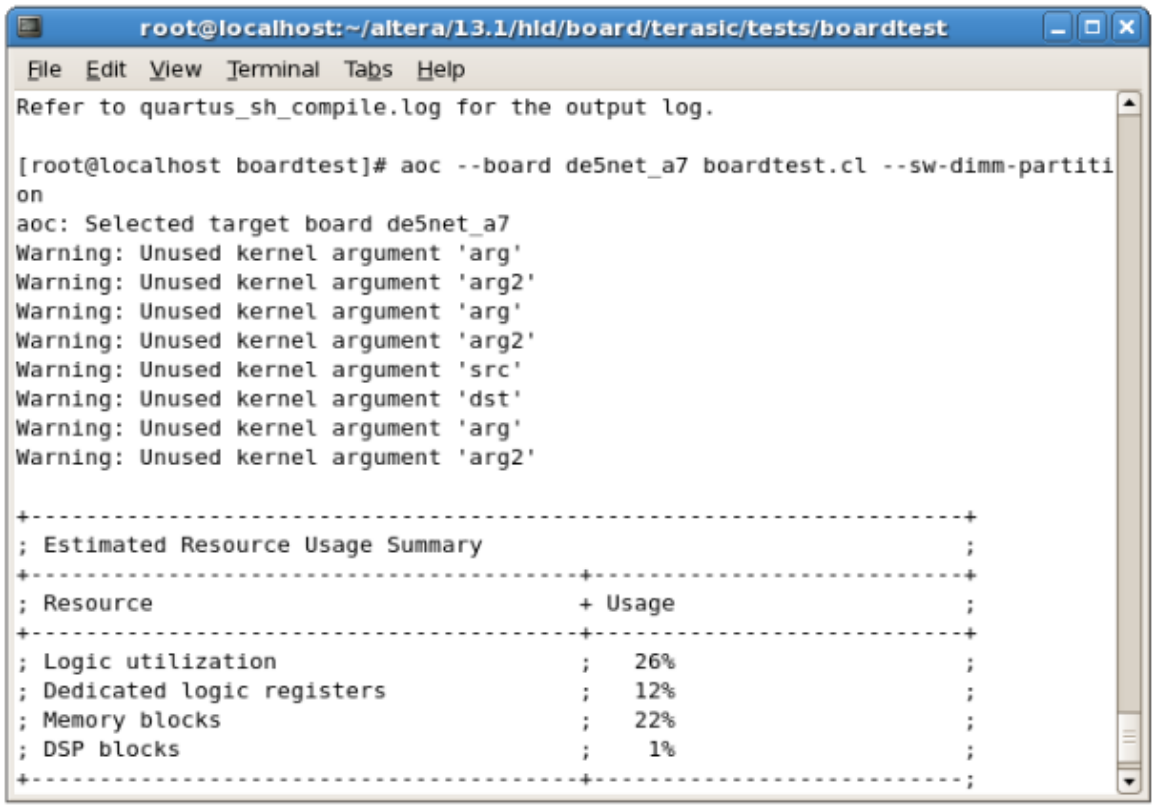

Figure 3-12 'aoc boardtest.cl" OpenCL kernel compile successfully

■ Compile Host Program

In the terminal, type *"cd /root/altera/13.1/hld/board/terasic/tests/boardtest"* and then type *"make -f Makefile.linux"* to compile the host program.

When build is successfully, you will see successful message as show in **Figure 3-13**. The execute file is generate in the same directory which named boardtest_host.

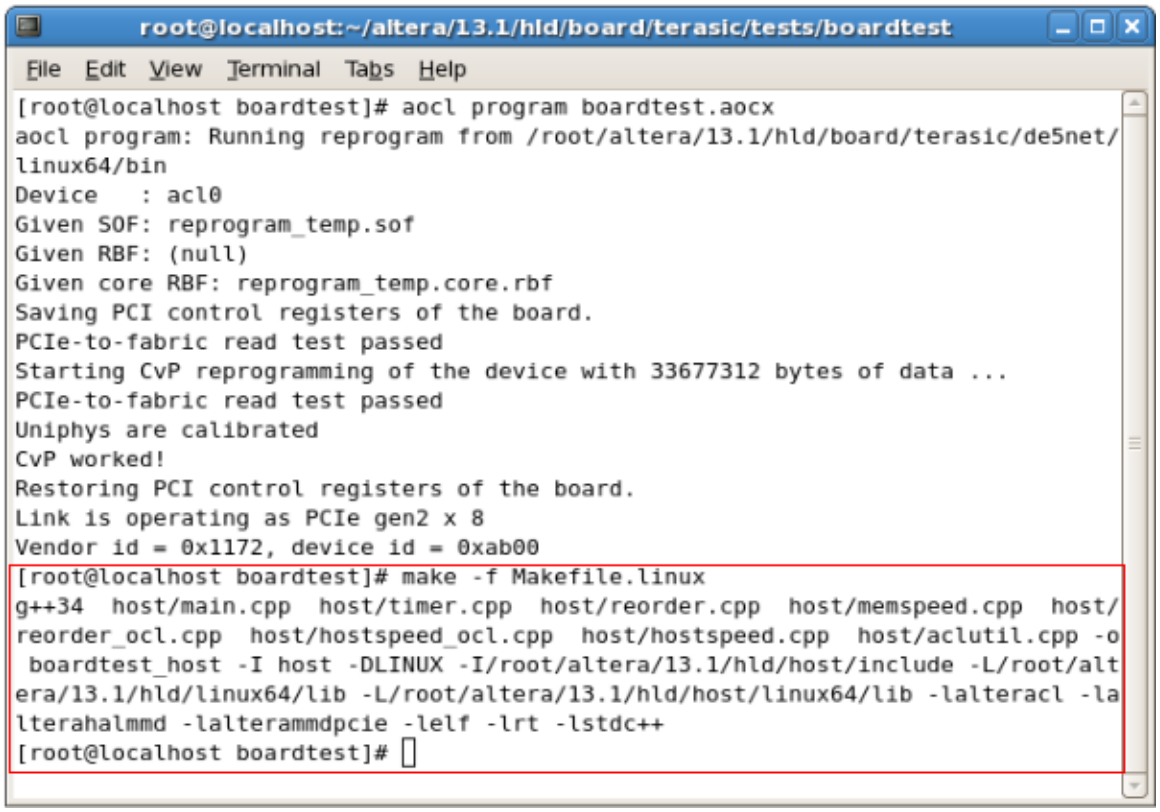

Figure 3-13 successful Message for boardtest Host Program build

■ Test boardtest project

Firstly, In the terminal, type "*cd /root/altera/13.1/hld/board/terasic/tests/boardtest*" to go to the **boardtest** project folder, then type "*aocl program boardtest.aocx*" to configure FPGA with the OpenCL Image boardtest.aocx.

Then, launch the compiled Host Program to start boardtest execute file for test. In the terminal type "./boardtest_host". **Figure 3-14** shows the execution is successful.

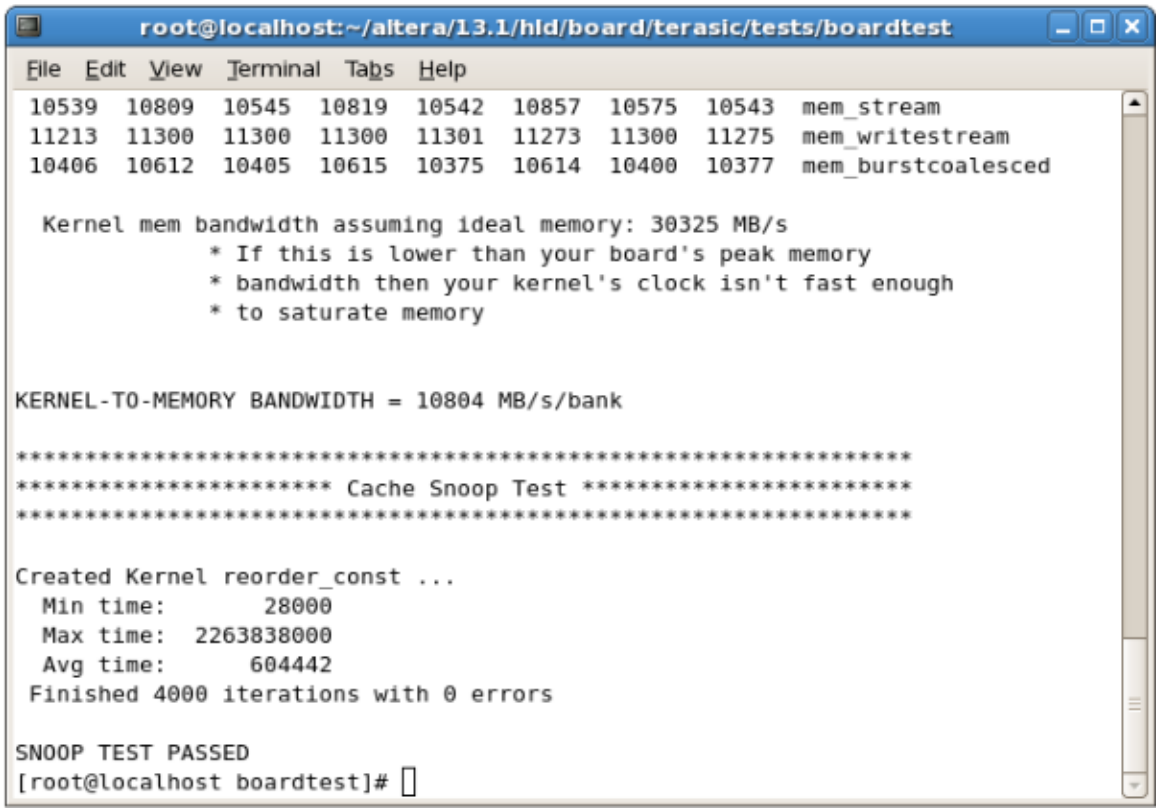

Figure 3-14 successful Message for "boardtest" test