

# Errata “Modern Digital Designs with EDA, VHDL and FPGA”

# Errata “Modern Digital Designs with EDA, VHDL and FPGA”

## Chapter 1

- Page 11, exercise problem 3, the 2nd line: “LEDs, SWs amd KEYs ...” should be “LEDs, SWs and KEYs...”.

## Chapter 3

- Page 95, exercise problem 12, the 2nd row of the table: x = ‘0’ should be x = ‘1’.

rst	Clk	X	C
1	↑	1	1011
0	↑	1	0110
0	↑	1	
0	↑	0	
0	↑	0	
0	↑	1	
0	↑	1	

- Page 94, exercise problem 6, the “OUT” in the VHDL codes should be “OUTPUT” (four places).

**--Version #1**

**If (A = ‘0’) then**

**Output <= X;**

**Elsif (B = ‘1’) then**

**Output <= Y;**

**End if;**

**--Version #2**

**If (A = ‘0’) then**

**Output <= X;**

**Else**

**If (B = ‘1’) then**

**Output <= Y;**

**End if;**

**End if;**

## Chapter 4

- Page 111, the “CASE-WHEN” codes were not aligned properly.
- Page 135, the 7th line from top:

## Errata “Modern Digital Designs with EDA, VHDL and FPGA”

```
LIBRARY IEEE;  
USE IEEE.numeric_std.all;
```

Should be

```
LIBRARY IEEE;  
USE IEEE.std_logic_1164.all;  
USE IEEE.numeric_std.all;
```

### Chapter 5

- Page 160, item 5 in the first paragraph of section 5.3.2: ”

Force “ack = ‘0’ when the “host” detects “ready = ‘0’.

Should be

Force “ack” = ‘0’ when the “host” detects “ready” = ‘0’.

- Page 166, the 23<sup>rd</sup> line:

```
If (code_fifo(15 downto 8) /= x"F0") then
```

Should be

```
if (code_fifo(7 downto 0) /= x"F0" and  
code_fifo(15 downto 8) /= x"F0") then  
disp_buf<= disp_buf(7 downto 0)  
    & scan_code;
```

- Page 185, exercise problem 16, the first line: “pre-define” should be “pre-**defined**”.

### Chapter 6

- Page 192, the 6th line from bottom: “(800 × 525) / 5MHz” should be “(800 × 525) / **25**MHz”.
- Page 193, the “ELSE” and “END IF” lines were not aligned properly.
- Page 225, the first line: “Animation with Keyboard Contrils” should be “Animation with Keyboard **Controls**”.
- Page 190, Table 6.2 should be:

## Errata “Modern Digital Designs with EDA, VHDL and FPGA”

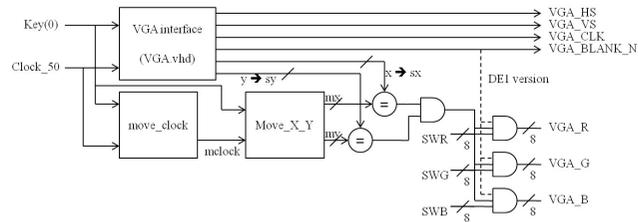
VGA mode		Horizontal Timing Specifications				
Configuration	Resolution(H×V)	a(μs)	b(μs)	c(μs)	d(μs)	Pixel clock (MHz)
VGA (60Hz)	640×480	3.8	1.9	25.4	0.6	640/c
VGA (85Hz)	640×480	1.6	2.2	17.8	1.6	640/c
S V G A (60Hz)	800×600	3.2	2.2	20.0	1.0	800/c
S V G A (75Hz)	800×600	1.6	3.2	16.2	0.3	800/c
S V G A (85Hz)	800×600	1.1	2.7	14.2	0.6	800/c
XGA (60Hz)	1024×768	2.1	2.5	15.8	0.4	1024/c
XGA (70Hz)	1024×768	1.8	1.9	13.7	0.3	1024/c
XGA (85Hz)	1024×768	1.0	2.2	10.8	0.5	1024/c
S X G A (60Hz)	1280×1024	1.0	2.3	11.9	0.4	1280/c

• Page 190, Table 6.3 should be:

VGA mode		Vertical Timing Specifications				Pixel clock (MHz)
Configuration	Resolution(H×V)	va(lines)	vb(lines)	vc(lines)	vd(lines)	
VGA (60Hz)	640×480	2	33	480	10	640/c
VGA (85Hz)	640×480	3	25	480	1	640/c
S V G A (60Hz)	800×600	4	23	600	1	800/c
S V G A (75Hz)	800×600	3	21	600	1	800/c
S V G A (85Hz)	800×600	3	27	600	1	800/c
XGA (60Hz)	1024×768	6	29	768	3	1024/c
XGA (70Hz)	1024×768	6	29	768	3	1024/c
XGA (85Hz)	1024×768	3	36	768	1	1024/c
S X G A (60Hz)	1280×1024	3	36	1024	1	1280/c

• Page 204, Figure 6.11: the bus widths for “y → sy”, “x → sx”, “my” and “mx” are all 8. The number 8 should be removed in all four places. The correct figure 6.11 is:

## Errata “Modern Digital Designs with EDA, VHDL and FPGA”



### Chapter 7

- Page 253, the 18th line: “X(9 downto 3 '&')” should be “X(9 downto 3)”.
- Page 276, the 5th line:

```
Port(  
    mem_out      : out    std_logic_vector(9 downto 0);
```

Should be

```
Port(  
    ... same as that in VGA_font except  
    mem_out      : out    std_logic_vector(9 downto 0);
```

- Page 291, the 3rd line: “IF ...” were not aligned properly.
- Page 248, the 7th line: “TX = X mod 8 and TY = Y mod 8...” should be “TX = X/8 and TY = Y/8...”
- Page 256, the 4th line of the high-level pseudo-code: “VRAM(y\*256 + x) = data” should be “VRAM(y\*128 + x) = data”.

### Chapter 8

- Page 297, the end of the 6th line: “RCA connectors” should be “phone jacks”.
- Page 309, the 22nd line comment: “-- send 2nd byte” should be “-- send 3rd byte”.
- Page 324, the 4th line of the 4th paragraph: “for an 4-bit number” should be “for a 4-bit unsigned number”.

## Errata “Modern Digital Designs with EDA, VHDL and FPGA”

### Chapter 9

- Page 360, the 9th line: “0 to CLOCK\_FREQ” should be “0 to **delay\_range**”.
- Page 360, the 24th line from bottom, “(delay count > CLOCK\_FREQ - 1)” should be “(delay count > **delay\_range** - 1)”.
- Page 362, the 2nd line: “(delay count > CLOCK\_FREQ - 1)” should be “(delay count > **delay\_range** - 1)”.
- Page 365, the 15th line of the first paragraph, “apply to bot boards” should be “apply to **both** boards”.
- Page 379, the 9th line from bottom: “the zoom factors” should be “the zoom **factor**”.
- Page 380, the 18th line comment: “(or a = a2 - b2 + mx)” should be “(or a = **a<sup>2</sup> - b<sup>2</sup> + mx**)”.
- Page 384, the 2nd line: “in a 32-bit unsigned number” should be “in a 32-bit **signed** number”.
- Page 391, the 9th line from bottom: “zero is ...” should be “**Zero** is ...”.
- Page 391, the 6th line from bottom: “Not-a-number (Nan)” should be “Not-a-number (**NaN**)”.