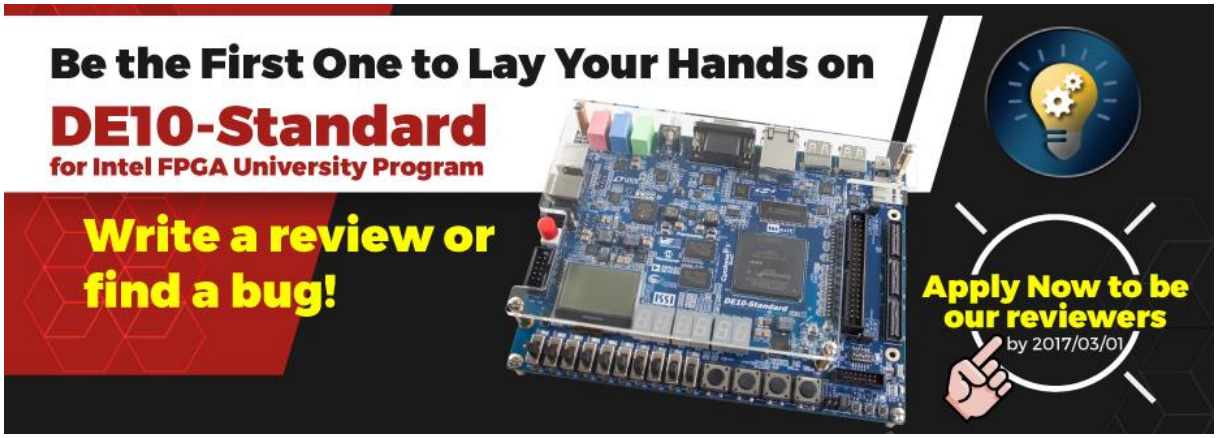

The DE10-Standard Kit is the new flagship for INTEL FPGA University Program, which will be widely used by preeminent universities and research institutes for teaching, inventions, research, as well as industrial applications.

DE series development & education board is the heart of Terasic and Intel FPGA University Porgram and the pilot for future FPGA designers and inventers. As a forefront FPGA developer in today's world, we value the reviews and feedbacks from our users and incorporate them into products' revisions and improvement.

With a keen intention to create a friendly environment to interact with Terasic board users, we would like to invite experienced FPGA designers who are "achievers and enthusiasts" from around the world to be our pilot users for the first DE10-Standard sample boards and provide us your esteemed feedbacks and opinions.

Candidate Criteria

We look for bright users with an unquenchable thirst for development and knowledge of FPGA design and a keen interest in exploring new field of possibilities for future path of FPGA. When submitting your application, tell us who you are and what you do in your own voice, not what you think we want to hear. Let us know why you want to be our reviewer of our new DE10-Standard Kit.

What to Present?

When writing your technical review for this event, keep in mind that what we are looking for is your own voice. It can be a description of a possible design you can develop with DE10-Standard, a comparison between this DE10-Standard to similar boards from other companies, a piece of advice or idea for future FPGA users, and last but not least, the technical properties of your review: that is, its breakthrough, the depth of technological examination, and degree of enhancement regarding DE10-Standard it contributes.

Project Schedule

02/22 – 03/01 Submit applications to be our reviewers
03/10 Announce the list of selected reviewers and Boards ship out
03/27 Submit Final Review
03/31 Announce the list of Cash Reward Winners

Your Job

You only need to provide a review article for the new DE10-Standard Kit

Rewards

Each selected reviewer will receive :

1. DE10-Standard Board
2. US$500
3. A Certificate of Excellence for contribution to Intel FPGA University Program
4. US$200 for each bug found

*Bug refers to a mistake found in board design that needs to be fixed via PCB layout change.
**The reward of bug-finding will be given to the reviewer who first reports the bugs. Terasic will list the reported bug(s) on this webpage, please report bug as soon as you find it to Ms. Elizabeth Chen at elizabeth@terasic.com.

Awarding Criteria

The best technical reviews are selected according to form, functional and emotional aspects; we will read the reviews for their degree of examination, qualities, functionality and usefulness in addition to ease of realization and realization efficiency, and human interaction.

Terasic offers expertise ranging from FPGA/ASIC board design, layout, to drivers, signal integrity analysis, and embedded system solutions. Our cutting-edge designs and manufacturing capabilities provide the state-of-the-art products and exceptional services to our esteemed customers. By working with world-renowned partners such as Intel, Cypress, Linear, ISSI, TI, Microchip and ADI, we continue to work in industry-leading technologies for future FPGA platforms and solutions. Choose Terasic, and see how we pave the fastest path to convert your concept into reality. We are your perfect partner in this highly competitive business world.