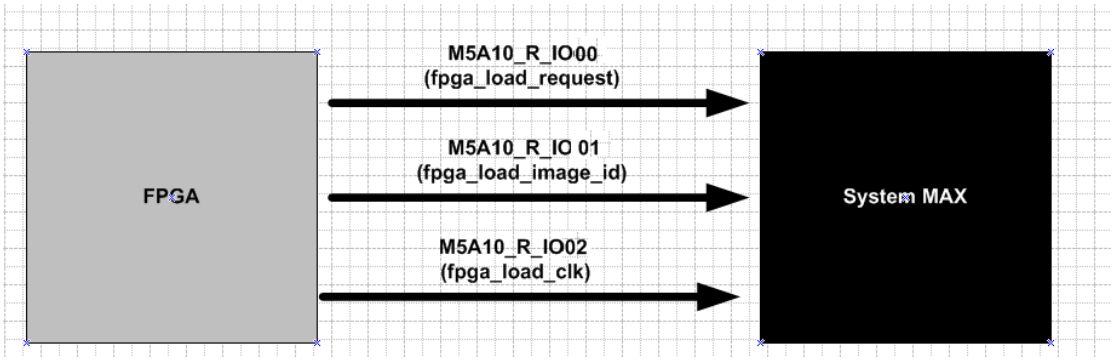
1. Block Diagram

   The FPGA can request system max to reconfigure FPGA via 3 I/O between FPGA and system max.

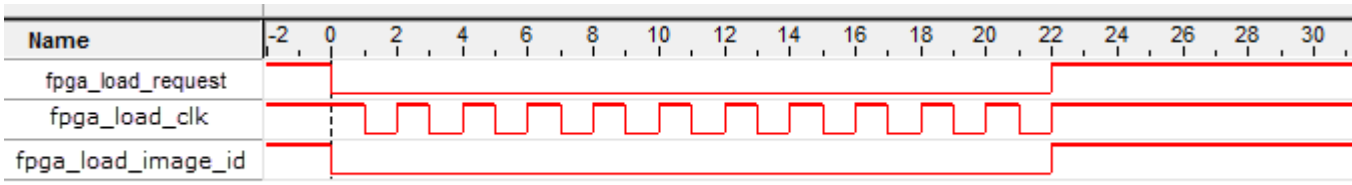


2. Function Table

Item	Signal Name	MAX I/O	FPGA Pin Assignment	System MAX Pin Assignment	Description for FPGA
1	fpga_load_request	M5A10_R_IO0[0]	AY36	R10	When the FPGA wishes to be reconfigured, this line will be pulled low ('0').This line will not be pulled high until the FPGA has been reconfigured. The CPLD should pass this through a dual-FF synchronizer, and sample several clock cycles (fpga_load_clk) of logic '0' before deciding to reconfigure the FPGA.
2	fpga_load_image_id	M5A10_R_IO0[1]	AY34	T10	This signal is sampled when a logic '0' is detected on the "fpga_load_request" signal. A value of '0' indicates the user image. A value of '1' indicates the default image. This value will be asserted at the same time as the "fpga_load_request" signal.
3	fpga_load_clk	M5A10_R_IO0[2]	BA34	T9	When the FPGA wishes to be reconfigured,this signal will output at

					leat 10 clock cycle (100Mhz) alone with "fpga_load_request " signal

3. Signal Waveform



4. FPGA control example code :

i. First, you must write both factory and user image to the FLASH.

ii. Download the .sof file of the example.

a. Turn the SW5 to the “0” position.

b. Press Button3.

c. You may see the FPGA board have been load into “User image”.

iii. Download the .sof file of the example.

a. Turn the SW5 to the “1” position.

b. Press Button3.

c. You may see the FPGA board have been load into “Factory image”.