7 Starting Your First HPS Design

Users can refer to the document My_First_HPS.pdf from the manual folder in the DE0-Nano-SoC System CD.

This document describes the complete C/C++ design flow, including:

1. Create and build a C/C++ project.
2. Copy files to Linux running on DE0-Nano-SoC.
3. Launch excutable files on Linux running on DE0-Nano-SoC.

8 Getting Help

For further discussion, support, and resources, please go to:

http://soc.terasic.com

9 What's different between the DE0-Nano-SoC kit and the Atlas-SoC kit?

The hardware is the same for the DE0-Nano-SoC kit and the Atlas-SoC kit. The only difference is the getting-started process for the two kits. Users can freely use the DE0-Nano-SoC kit resources on the Atlas-SoC kit and vice versa.

For more details on the Atlas-SoC kit, please visit:

http://www.rocketboards.org/atlas-soc

If you encounter any problems, please contact us via

Email: support@terasic.com Tel: +886-3-575-0880

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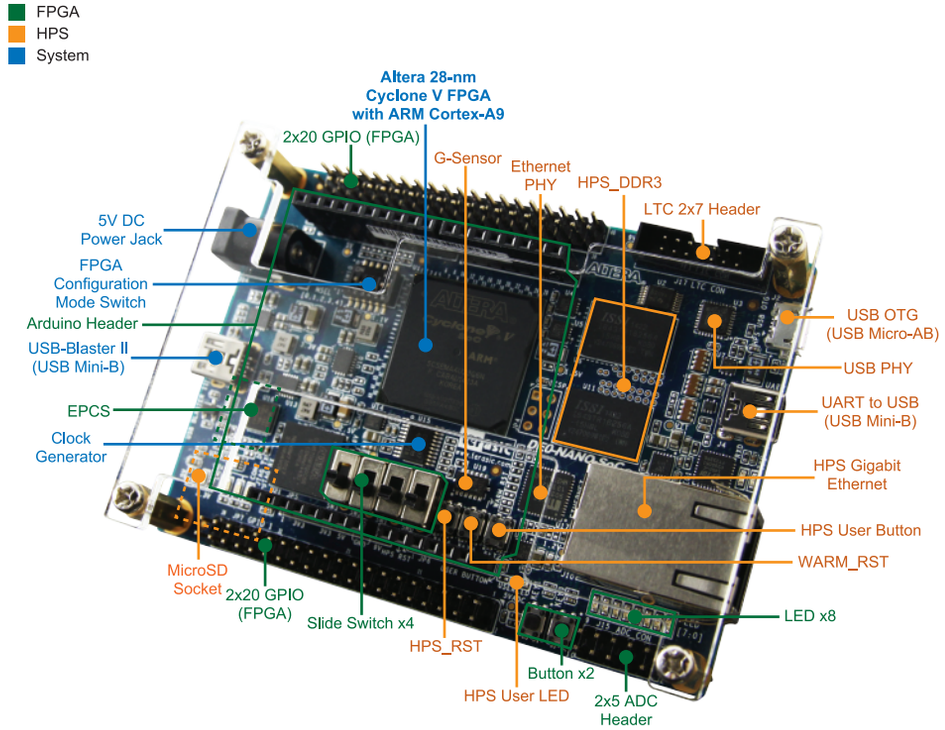
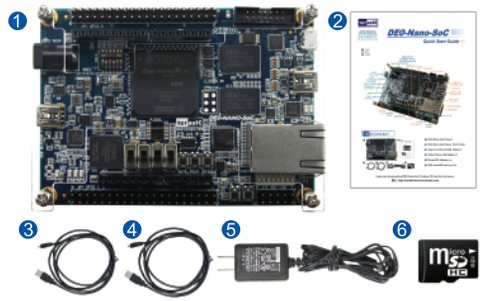
ALTERA UNIVERSITY PROGRAM

DE0-Nano-SoC

Quick Start Guide



1 What's in the Box?

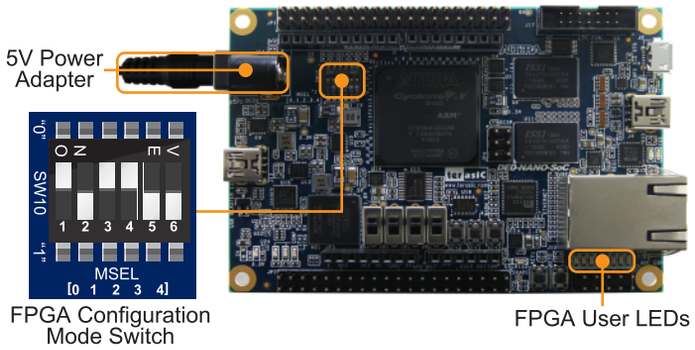


1. DE0-Nano-SoC Board
2. DE0-Nano-SoC Quick Start Guide
3. Type A to Mini-B USB Cable x1
4. Type A to Micro-B USB Cable x1
5. Power DC Adapter (5V)
6. microSD card (installed)

Users can download the DE0-Nano-SoC System CD from the link below:

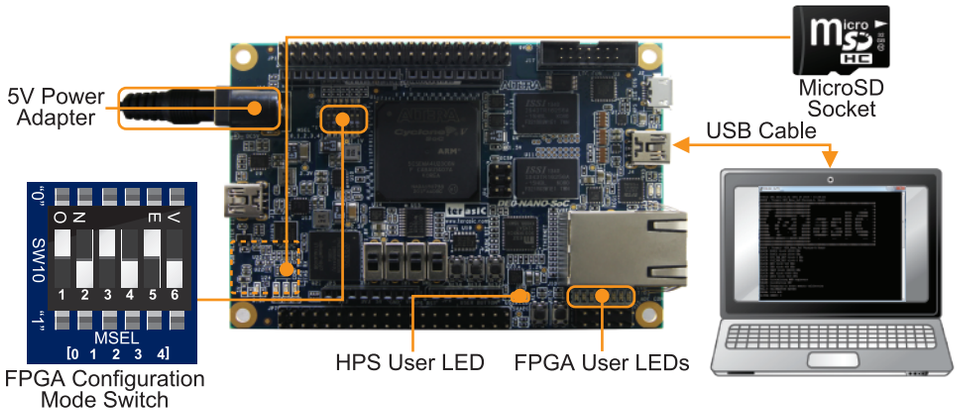
http://soc.terasic.com

2 Performing Power-on Test: FPGA Configuration



1. Set the MSEL[4:0]= 10010 in Fast AS Mode.
2. Connect the power adapter to the power jack on the DE0-Nano-SoC.
3. All the FPGA user LEDs will be flashing.

3 Performing Power-on Test: HPS Boot First (Linux)



1. Set the MSEL[4:0] = 01010 to boot the DE0-Nano-SoC board from microSD card in FPPx32 mode.
2. Please makes sure the microSD card included in the kit has been inserted properly.
3. Connect the power adapter to the power jack on the DE0-Nano-SoC.
4. Users can observe the Linux booting message in UART terminal by connecting a USB cable between DE0-Nano-SoC and the host PC. For more details, please refer to the **Getting Started Guide** in the system CD.
5. The FPGA will be configured in U-Boot and all the FPGA user LEDs will be flashing.
6. After Linux boot is successful, users will see the HPS user LEDs blinking for a while.
7. If UART terminal is launched, users can type "root" in the terminal to login Linux.

4 Contents of DE0-Nano-SoC System CD

Users can download the DE0-Nano-SoC System CD from the link below:

http://soc.terasic.com

DE0-Nano-SoC System CD Contents	
Directory Name	***Contents***
Manual	Contains the DE0-Nano-SoC documentations
Demonstrations	Contains design examples for DE0-Nano-SoC
Datasheet	Contains the datasheets of components on the DE0-Nano-SoC
Schematic	Constains the schematic of DE0-Nano-SoC
Tools	Contains the design tools for DE0-Nano-SoC

5 Getting Started with the DE0-Nano-SoC Board

Users can refer to the document Getting_Started_Guide.pdf found in the DE0-Nano-SoC System CD manual folder.This guide contains a quick overview on the hardware and software setup including step-by-step procedures from installing the necessary software tools to using the DE0-Nano-SoC board.

The main topics that this guide covers are listed below:

1. Software Installation: Quartus II and EDS.
2. Development Board Setup: Power up the DE0-Nano-SoC.
3. Perform FPGA System Test: Download a FPGA SRAM Objective File (.sof).
4. Running Linux on DE0-Nano-SoC Board.

6 Starting Your First FPGA Design

Users can refer to the document My_First_FPGA.pdf from the manual folder in the DE0-Nano-SoC System CD.

This document describes the complete FPGA design flow, including:

1. Create a new Quartus II project.
2. Add user logic and utilize MegaCore IPs.
3. Download a .sof file to the FPGA to view the result.